Design and Implementation of a Transformerless Single-Stage Single-Switch Double-Buck Converter With Low DC-link Voltage, High Step-Down, and Constant Input Power Factor Features

Yu Chen, *Member, IEEE*, Zhihao Zhong, and Yong Kang

***Abstract*—This paper presents a new transformerless single-stage single-switch (S4) converter which integrates a buck-type power factor correction cell with a buck-type dc–dc output cell in a special way. The proposed converter preserves the advantages of existing transformerless S4 converters, such as the low voltage stress across the dc-link capacitor, low current stress of the switch, and high step-down input-to-output voltage. Moreover, the proposed converter provides a new attractive feature, i.e., its input power factor always keeps constant even when the line- and load-conditions vary. These characteristics make the proposed converter cost-efficient, easy-to-design, and suitable for the low-power and nonisolated applications. The principle and analysis of the proposed converter are presented in this paper, and a design example is also given to show the validity of analysis.**

***Index Terms*—LED driver, power electronics, power factor correction (PFC), single-stage single-switch (S4) converter.**

I. Introduction

MANY industrial applications require not only a tight dc voltage to feed their loads, but also a high-input power factor (PF) to reduce harmonic distortion in the current drawn from the grid. These requirements can be simply satisfied by a single power factor correction (PFC) converter [1]–[8]. However, its output voltage has the high ripples at twice of the line frequency. These ripples get even higher when the output voltage becomes lower and the load becomes heavier. The other solution is using a PFC converter in cascade with a dc–dc converter, with which the instantaneous input power and the stable output power can be decoupled by an intermediate dc-link capacitor [9]–[13]. However, such a two-stage configuration suffers from the increased component count, high cost, and complicated control.

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The authors are with the State Key Laboratory of Advanced Electromagnetic Engineering and Technology and the School of Electrical and Electronic Engineering, Huazhong University of Science and Technology, Wuhan 430074, China (e-mail: ayu03@163.com; cobeam@163.com; ykang@hust.edu.cn).

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To compromise the size, cost, and performance, many single-stage single-switch (S4) converters have been proposed. From the topology point of view, S4 converters can be treated as an integration version of the two-stage structure, in which the switches in the PFC and dc–dc converter are combined as one. Several advantages can be obtained using this integration approach: 1) the PFC and dc–dc cells share one switch, the size and cost can be reduced; 2) the high input PF can be obtained automatically by the PFC cell with the discontinuous conduction mode (DCM), only the output voltage needs to be regulated, the controller can be simple; and 3) the input and output power can still be decoupled since the intermediate dc-link capacitor is remained, therefore the voltage ripples in the output are alleviated. Due to these features, S4 converters are especially suitable for the low-power applications with critical size and cost limitations.

S4 converters with galvanic isolation have been well studied in the past decades [14]–[29]. However, in some lighting applications, galvanic isolation is not mandatory by the safety requirements or standards. For example, the driver for emerging solid-state lighting could be nonisolated, as the existing incandescent lamps are also not isolated from the grid [2], [30]–[32]. In such a case, transformerless S4 converters are more compact and cost-efficient solutions. Unfortunately, if a low output voltage is needed, an extremely narrow duty cycle is required in such kind of converters without utilizing a transformer, especially in the high-line condition. The narrow duty cycle is hard to be realized by a low-cost PWM controller and leads to a poor efficiency [3], [33], [34]. Therefore, the topology design for such transformerless S4 converters should compromise not only a good input PF and a stable output voltage, but also a high-voltage step-down feature (i.e., a low output voltage but a relatively large duty cycle).

Recently, several transformerless S4 converters have been presented to meet the aforementioned requirements. The boost/buck-boost S4 converter is presented in [35]. The boost PFC cell provides a good input PF, but it also requires a high dc-link voltage, which degrades the converter's step-down feature. The S4 converters with buck-boost PFC cells [33], [34], [36] reduce the dc-link voltage, and the voltage step-down can be realized by a buck [34], quadratic buck [33], or buck-boost [36] cell. However, the single switch in the aforementioned converters needs to handle the currents of both cells, which leads to the thermal problem of the switch. In [37] and [38], a buck/

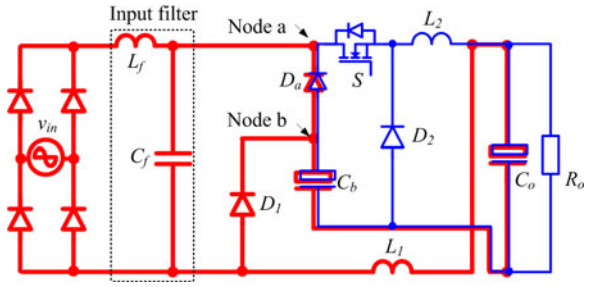

Fig. 1. Proposed transformerless S4 converter.

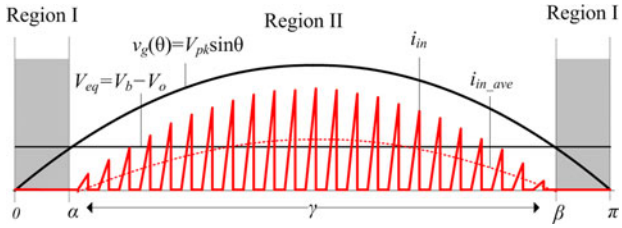

Fig. 2. Two working regions of the proposed S4 converter.

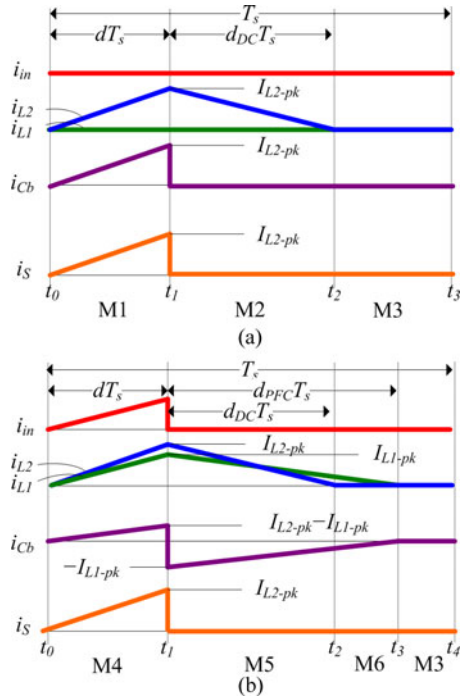

Fig. 3. Key waveforms of the proposed S4 converter: (a) in region I and (b) in region II.

buck-boost S4 converter is proposed to further reduce the dc-link voltage and enhance the step-down feature, and the single-switch does not need to handle the currents of both cells. However, since its PFC cell is buck type, the circuit must be carefully designed so that a satisfactory input PF can be obtained in the case of the line- and load-conditions variation.

To overcome the drawbacks of the aforementioned transformerless S4 converter but preserve their advantages, this paper proposes a new topology that integrates a buck PFC and buck dc–dc cells, as shown in Fig. 1. A buck dc–dc cell is embedded in the circuit (the components highlighted in blue), where the dc-link capacitor C_b is treated as its input; on the other hand, if S is turned ON and D_a keeps conducting (the conduction of D_a will be guaranteed by the parameter design, as discussed later), node a and node b would have the same voltage potential, the components in red construct an equivalent buck PFC cell, in which $v_{\rm in}$ is treated as input, C_b in series with C_o is treated as output. With such integration, the following benefits can be obtained:

1) the equivalent buck PFC leads to a low voltage stress across the dc-link capacitor C_b, the electrolytic capacitors with low voltage rating but large capacity can be used;
2) the single switch S needs to handle only the current of the dc–dc cell, the current stress is low;
3) integration of two buck cells leads to the high step-down input-to-output voltage;
4) for the equivalent buck PFC cell, its equivalent sink, C_b and C_o, in series with the reversed polarities. This structure brings in an attractive constant PF feature, which is independent of the line- and load-conditions. This unique feature facilitates the circuit design a lot.

To clearly explain the aforementioned characteristics, the operational modes of the proposed S4 converter are presented in Section II. Then, the circuit characteristics are analyzed in Section III. According to the analysis, an easy-to-follow design procedure, a design example, and its experimental results are given in Section IV. The conclusions are finally given in Section V.

II. Operational Modes of the Proposed S4 Converter

A. Definitions of Region I and Region II

To simplify the analysis, all components are treated as ideal; the dc link and output capacitors are large enough, therefore their voltage V_b and V_o are treated as constant within half of line-cycle period; and after the rectifier, the input voltage $v_{\rm in}$ has been rectified as $v_g(\theta)=|v_{\rm in}|=|V_{\rm pk}\sin\theta|$, where $V_{\rm pk}$ is the peak voltage of $v_{\rm in}$, and θ is a variable value from 0 to 2π. Especially, considering half of line-cycle from 0 to π, $v_g(\theta)$ can be expressed as

$$v_g(\theta)=|v_{\rm in}|=V_{\rm pk}\sin\theta \qquad \theta\in[0,\pi]\,. \tag{1a}$$

The proposed S4 converter includes a buck-type PFC cell, therefore, two working regions can be found within half of line-cycle period, as shown in Fig. 2. With the proposed integration, the equivalent voltage $V_{\rm eq}=V_b-V_o$ acts as the sink of the PFC cell, the rectifier does not conduct when $v_g(\theta)<V_{\rm eq}$, this interval is defined as Region I. Oppositely, if $v_g(\theta)>V_{\rm eq}$, the rectifier conducts and a input current $i_{\rm in}$ appears. This interval is defined as Region II. The start point α and end point β of Region II have been marked in Fig. 2, they can be expressed as

$$\alpha=\arcsin\frac{V_{\rm eq}}{V_{\rm pk}} \text{ and } \beta=\pi-\arcsin\frac{V_{\rm eq}}{V_{\rm pk}}. \tag{1b}$$