New CMOS Inverter-Based Voltage Multipliers

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Abstract —**Four new CMOS inverter-based voltage multipliers consisted of PMOS/NMOS pass transistors, inverter circuits, and capacitors are proposed in the paper. The proposed voltage multipliers which combine the functions of rectifiers and charge-pumps improve the power conversion efficiency and reduce the number of passive components therefore they are suitable for the integration. The voltage multiplier with positive output voltage is implemented with TSMC 0.35μm CMOS 2P4M processes, and the experimental results have showed good agreement with the theoretical analysis. The chip area without pads is only 1.75×1.32 mm^2 for five-stage positive output voltage of voltage multiplier.**

I. INTRODUCTION

More and more applications of voltage multipliers in different fields can be found in many literatures. An AC/DC charge-pump, sometimes also called the voltage multiplier, converts the received AC input voltage to a constant DC output voltage with amplitude multiplication. Due to its easy architecture and suitable conversion performance, the rectifier circuits have been widely used in Radio Frequency Identification (RFID), wireless telemetry, biomedical implants and other applications [1-3].

To realize AC/DC conversion, the conventional full-wave rectifiers consisted of diode-connected NMOS and PMOS transistors suffers from the power loss due to the intrinsic threshold voltage [4]. It is usually used in high voltage circuits where the diode forward voltage drop is relatively low. However, for low voltage rectifiers, this dropout voltage is significantly large and proportional to the conduction current. It degrades the rectified output voltage and power conversion efficiency (PCE). To enhance the efficiency of the rectifier, an active rectifier with low dropout voltage is presented in [5]. But more MOS transistors are used in [5]. Active diode [6] is another solution to reduce the forward threshold voltage. In [6], it allows the current to flow in only one direction through the device and has a low dropout voltage across it. However, it is difficult to operate in a high frequency range owing to its circuit complexity. The voltage drop of the diode-connected NMOS transistor can be reduced by adding an external threshold voltage cancellation circuit to compensate the threshold voltage drop by applying an external bias voltage in [7]. In [8], two diodes of the full-wave rectifier are replaced using two cross-coupled PMOS transistors. Nevertheless, the bottom two diodes are still realized by NMOS diodes to block the reverse current, so the efficiency is not optimal. A low-loss CMOS full-wave active rectifier is presented in [9]. It is composed of two dynamically biased and symmetrically matched active diodes realized by an NMOS switch and driven by a comparator. In [10], the four-transistor cell self-driven synchronous rectifier with the floating-gate version is reported. This technique allows independently program NMOS and PMOS threshold voltages by depositing charge on the floating gates. But the complicated control circuits are needed in [9] and [10].

Consequently, we propose new area-aware AC/DC architectures, which use PMOS/NMOS pass transistors, inverter circuits, and one capacitor in the single-stage rectifier. The multi-stage charge-pump rectifier can be performed using the stacked architecture. In this paper, the circuit description of proposed positive-voltage single-stage AC/DC converter is discussed in sections II. Section III presents the positive-voltage charge-pump rectifiers. The experimental result of proposed charge-pump rectifiers is presented in section IV, and the conclusion is made in section V.

II. PROPOSED POSITIVE-VOLTAGE SINGLE-STAGE RECTIFIER

The proposed positive-voltage single-stage rectifier circuit is shown in Fig. 1(a), and its block diagram is shown in Fig. 1(b). It consists of PMOS pass transistor (M_{P1}), dynamic switching circuits (M_{IP1} and M_{IN1}), and one capacitor (C_1). The input terminal V_i is connected directly or via a resonance tuning circuit to the coil.

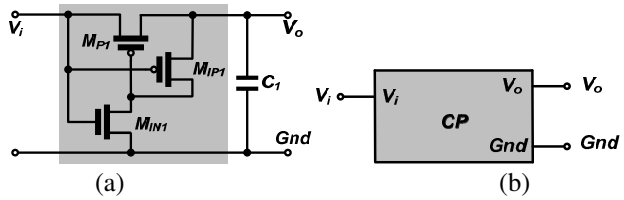

Fig. 1. Proposed positive-voltage single-stage rectifier (a) circuit (b) block diagram.

The operational principles of proposed positive-voltage single-stage rectifier circuit are shown in Figs. 2(a) and 2(b) for positive phase as $V_i > 0$, and negative phase as $V_i < 0$, respectively. The input and output waveforms are illustrated for the time domain in every cycle shown in Fig. 2(c). The peak-to-peak amplitude of square wave is $2V_{ref}$. In the positive phase, the transistors M_{P1} and M_{IN1} operated in the triode region are ON, and M_{IP1} is OFF in the cutoff region. The current I_O flows from V_i to charge the capacitor C_1. In the negative phase, the transistors M_{P1} and M_{IN1} operated in the

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cutoff region is OFF, and M_{IP1} is ON in the triode region. The C_1 holds the charging voltage in the negative phase, because M_{IP1} is connected between the gate and source of the M_{P1} transistor. This technique provides no DC current path from the gate of M_{P1} to ground, therefore there is no leakage current flowing to ground. When V_i is higher than V_o, the charging is continued until V_o equals to the maximum output voltage V_{ref}.

The factual charge transfer process is much more complicated, because the MOS transistors actually work in different regions in every cycle [11-12]. Here, we study the basic single-stage rectifier in different input waves including square wave and sine wave. The M_{IP1} and M_{IN1} are assumed as ideal switch models in the single-stage rectifier shown in the Figs. 3(a) and 3(b), and the transistor current is assumed to be equal to the DC loading current.

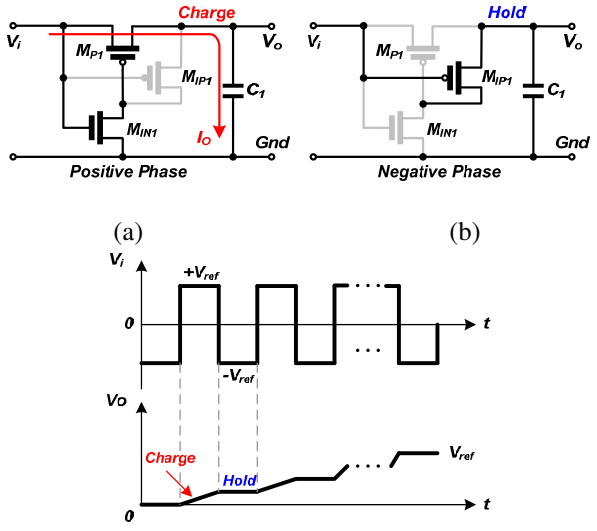

Fig. 2. Operation of positive-voltage single-stage rectifier (a) positive phase (b) negative phase (c) input/output waveforms.

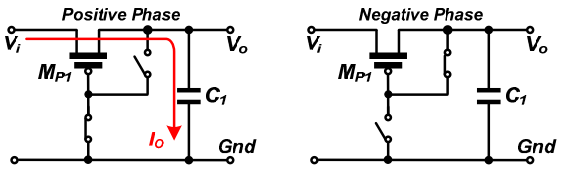

Fig. 3. Model of positive-voltage single-stage rectifier (a) positive phase (b) negative phase.

III. PROPOSED POSITIVE-VOLTAGE CHARGE-PUMP RECTIFIERS

To further increase the DC output voltage, an N-stage voltage multiplier is typically employed at constant input power, roughly N times larger than that achievable with a single-stage. The proposed positive-voltage three-stage charge-pump rectifier circuit which includes three stacked single-stage rectifiers is shown in Fig. 4. In the state 1, the PMOS pass transistors M_{P1} conducts the charging current to the capacitor C_1 in positive phase. The transistors M_{P1} and M_{IN1} operated in the triode region are turned on, and M_{IP1} is turned off in the cutoff region. The maximum output voltage of C_1 is V_{ref}. Next, in the state 2, when V_{in} is in negative phase, the voltages of C_1 and V_{in} are transferred to C_2 via M_{P2}. The transistors M_{P2} and M_{IN2} are turned on and operated in the triode region, and M_{IP2} operated in the cutoff region is turned off. The maximum output voltage between two terminals of C_2 is $2V_{ref}$. When V_{in} is in positive phase again, that is, in the state 3, the voltages of C_2 and V_{in} are transferred to C_3 via M_{P3}. The transistors M_{P3} and M_{IN3} operated in the triode region are turned on, and M_{IP3} is OFF operated in the cutoff region. The maximum output voltage between two terminals of C_3 is $2V_{ref}$. So the maximum output voltage V_{out} via C_1 and C_3 to ground is $3V_{ref}$. Since the PMOS pass transistors M_{P1}-M_{P3} have the leakage currents when they are turned off, the dynamic switching circuits (M_{IP1}-M_{IP3} and M_{IN1}-M_{IN3}) are designed to compensate the voltage drops caused by the leakage currents.

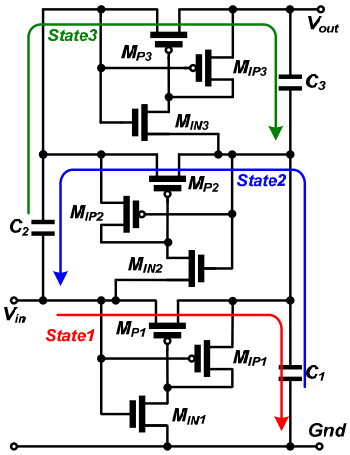

Fig. 4. Proposed positive-voltage three-stage charge- pump rectifier.

The proposed positive-voltage five-stage charge-pump rectifier circuit which includes five stacked single-stage rectifiers is shown in Figs. 5(a)~5(d) with four types. First, type I in Fig. 5(a) shows the five stacked single-stage rectifiers directly connected together as in Fig. 4 of three-stage charge-pump rectifier. The operational principle of Fig. 5(a) is the same as the three-stage one. The PMOS pass transistors are M_{P1}-M_{P5}. First, when V_{in} is in positive phase, the charging currents are transferred to capacitors C_1, C_3 and C_5 through M_{P1}, M_{P3}, and M_{P5}, respectively. Next, when V_{in} is in negative phase, the voltages of C_1 and V_{in} are transferred to C_2 via M_{P2}, and the voltages of C_1, C_3 and V_{in} are transferred to C_4 via M_{P4}. Both of the maximum output voltages between two terminals of C_2 and C_4 are $2V_{ref}$. The maximum output voltages between two terminals of C_1, C_3 and C_5 are V_{ref}, $2V_{ref}$, and $2V_{ref}$, respectively. So the maximum output voltage V_{out} via C_1, C_3 and C_5 to ground is $5V_{ref}$.