New Subthreshold Concepts in 65nm CMOS Technology

Farshad Moradi[1], Dag T. Wisland[1], Hamid Mahmoodi[2], Ali Peiravi[3], Snorre Aunet[1], Tuan Vu Cao[1]
[1]Nanoelectronics Group, Department of Informatics, University of Oslo, NO-0316 Oslo, NORWAY
[2]School of Engineering San Francisco State University, San Francisco, CA 94132, USA
[3]School of Engineering, Ferdowsi University of Mashhad, Mashhad, IRAN
Emails: [1]{moradi, dagwis}@ifi.uio.no,[2]mahmoodi@sfsu.edu, [3]peiravi@ ferdowsi.um.ac.ir

Abstract

In this paper challenges observed in 65nm technology for circuits utilizing subthreshold region operation are presented. Different circuits are analyzed and simulated for ultra low supply voltages to find the best topology for subthreshold operation. To support the theoretical discussions different topologies are analyzed and simulated. Various aspects of flip-flop circuits are described in detail to study which topology would be most suitable for ultra low supply voltage and low-power applications. Simulation results show that the power consumption decreases by at least 23% compared with other flip-flops. Also, the setup time and the hold time are improved.

Keywords

Low-voltage, low-power, subthreshold, nanoscale

1. Introduction

In the last few years, large efforts have been made in research and development on low energy circuits for battery operated wireless sensor nodes. Recently a number of papers reporting ADC's utilizing time-domain instead of amplitude domain have been reported [1]-[4]. This class of converters may be built entirely of digital components, but this would put strict requirements on the comparator and sampling circuitry. To meet these requirements low power and high speed flip-flops with a sufficiently low possibility for metastability must be designed. Recently, as we approach atomic scale devices, leakage currents have increased dramatically, leading to higher static power dissipation. Therefore, leakage must be taken into consideration when evaluating these circuits since it has become a significant contributor to the overall power consumption in deep-submicron CMOS processes

Sub-threshold current rises due to lowering of threshold voltage which is scaled down to maintain transistor ON current in the face of falling power supply voltage. Voltage scaling for standby power reduction was suggested since both subthreshold current and gate current decrease dramatically (with V^4 for gate leakage) [5]. Lowering supply voltage thus saves standby power by decreasing both standby current and voltage [6]. The subthreshold region (weak inversion) is often utilized to implement power efficient circuits for ultra low power wireless applications, but due to the much lower current in subthreshold region compared with higher supply voltages, the evaluation speed of such circuits operating in weak inversion is decreased. Therefore, new techniques to improve circuit speed need to be developed.

The rest of the paper is organized as follows. In section 2, some characteristics of 65nm CMOS technology in weak inversion are described. Also the effect of some techniques in subthreshold region is explained in details. In section 3, new flip-flop design concepts in 65 nm CMOS technology for operation in subthreshold region are proposed by improving upon existing designs. The comparison of results is also included in this section. Conclusions are presented in section 4.

2. Subthreshold 65nm characteristics

Subthreshold design has emerged as a good potential for ultra low power applications such as wireless sensor networks, medical instruments, and portable devices.

We have observed some specific behaviors from devices operating in subthreshold region in the 65nm technology due to lack of well-engineered models for subthreshold region. Short channel devices have been optimized for regular strong inversion circuits to meet various objectives such as high mobility, reduced DIBL, low leakage current, and minimal Vth roll-off. However, a transistor that is optimized for operating in superthreshold logics are not necessarily optimal in low voltage, low power dissipation applications designed for operation in the subthreshold region. Optimization problems include the transistor sizing, the drive current for PMOS and NMOS devices, the effects of some techniques such as Forward Body Bias (FBB), Reverse Body Bias (RBB), and stacking effects on threshold voltage and drive current. Although it would be ideal to have a dedicated process technology optimized for subthreshold circuits this is not practically achievable. In order to design optimal subthreshold circuits using CMOS devices that are targeted for superthreshold operation, it is crucial to develop design techniques that can utilize the side effects that appear in this new regime. However, in the absence of such a dedicated process the development of low voltage low power applications using the 65nm CMOS technology requires care and novelty in design.

2.1 DC Analysis

In this section three topologies for basic circuits are presented and simulated using DC analysis. Fig.1 illustrates the topologies that are simulated in 65nm technology with supply voltage equal to VDD=0.9V. In all topologies minimum sizes for the transistors are used. Fig.1 (a) shows the three stacked devices (two PMOS and one NMOS referred to as 2PMOS). Fig.1 (b, c) are referred to as 3PMOS and 2NMOS respectively. Simulation results based on DC analysis for these three configurations are illustrated in Fig. 2. As it can be observed, the short circuit current in 2NMOS is higher than for the other circuits, which implies that the delay for 2NMOS is higher than for the other topologies causing increased short circuit current through this circuit.

2.2 Stacking effect in 65nm Technology

Stacking has been proposed as a technique to decrease the leakage current in subthreshold region [7]. This technique is based on increasing the threshold voltage of source to bulk as a result of which the threshold voltage will increase thereby reducing leakage current in idle mode. However, when the circuits are forced to work at ultra low supply voltage (subthreshold region), increased subthreshold current is desired to improve the circuits speed. In order to find better circuit topologies which use the stacking technique, two topologies which utilize the stacking effect are simulated.

As known, in CMOS technologies, the speed of the NMOS is higher than PMOS because of higher mobility of electrons compared with holes, but simulations show that for 65nm technology in ultra low supply voltages (in subthreshold), this behavior is changed. The main reason for this phenomenon is that these models are engineered for superthreshold circuits. For superthreshold applications, the threshold voltage of PMOS devices are lowered to compensate the effect of lower mobility compared to NMOS devices. But in subthreshold region, the exponential dependence of subthreshold current to Vth causes some unexpected results [8]-[10]. Fig.3 shows two topologies used to illustrate the stacking effect on speed. These two circuits were simulated for ultra low supply voltages (VDD=0.2V) to investigate which is the faster topology. Two similar pulses are applied to the inputs of the circuits, and the charging and discharging speeds of the output nodes are considered and compared for Circuit1 and Circuit2, respectively. Fig.4 shows

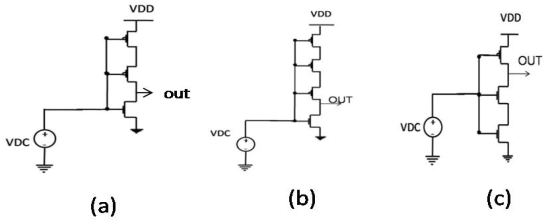

Figure 1: (a) 2PMOS (b) 3PMOS (c) 2NMOS circuits.

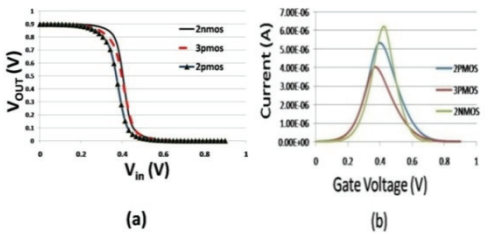

Figure 2: (a) V_{out} vs. Vin (b) IDS current vs. gate voltage.

the simulation results for these two configurations, which show that Circuit1 has a higher speed compared with Circuit2 at ultra low supply voltages, so employing Circuit1 configuration in circuits such as D-Flip-flops instead of the Circuit2 topology, gives much better results. To attain the same speed for Circuit2, the NMOS transistors must be upsized 13 times, so the area overhead of Circuit2 is higher than Circuit1 in the same speed. Based on this concept the SAFF (Sense amplifier flip-flop) and the HLFF (Hybrid latch flip flop) are simulated using the complementary circuits of the NMOS stacked transistors configuration. Results of simulation utilizing Circuit1 topology show that higher operating speeds are achievable at lower supply voltages as a result of which we attain significant reduction in power dissipation. Fig.5 shows the effect of body biasing technique on an inverter with different bulk voltages.

3. Flip-flops in subthreshold

3.1 Hybrid Latch Flip Flop

The Hybrid-latch flip-flop (HLFF) (Fig. 6), presented in [12] is one of the fastest structures presented. It also has a very small PDP [13]. The major advantage of this structure is its soft-edge property, i.e., its robustness to clock skew. One of the major drawbacks of the hybrid design in general is the positive hold time, discussed in Section II-B. Due to the single-output design, the power-consumption range of the HLFF is comparable with that of the static circuits. However, depending on the data pattern, the precharged structures can dissipate more than static structures for data patterns with more "ones".

Hybrid design appears to be very suitable for high performance systems with little or no penalty in power when compared to classical static structures. As it can be seen in the HLFF circuit, there are stacked NMOS transistors that must evaluate the state of the circuit during the delay for three series inverters. As explained in the previous section, three stacked NMOS configuration has a lower speed than three stacked PMOS transistors in subthreshold region.

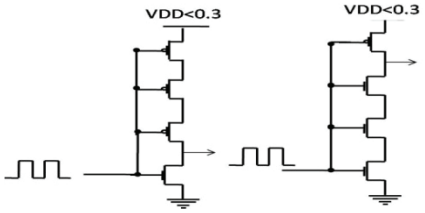

Figure 3: (a) Circuit1 (b) Circuit2 schematics.

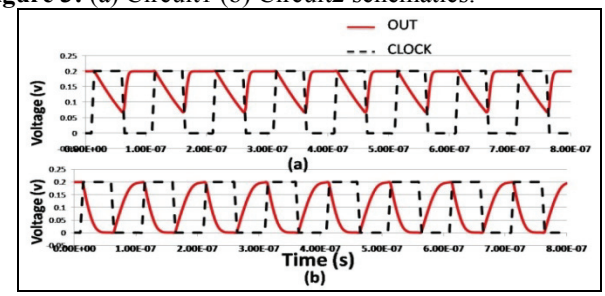

Figure 4: Transient analysis for (a) Circuit2 (b) Circuit1 (with minimum size for all transistors in 27°C, TT model).

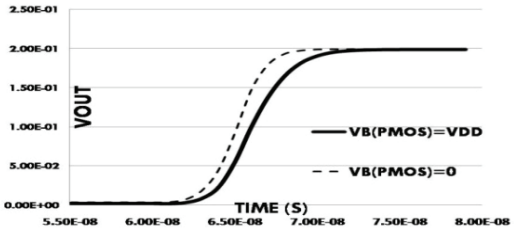

Figure 5: The effect of body biasing technique.