Modeling and Design of GaAs MESFET Control Devices for Broad-Band Applications

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Abstract — **In this paper, closed-form expressions are developed for the small-signal parameters of broad-band GaAs control MESFET's. The theoretical conducting-state resistance and nonconducting-state capacitance are compared with experimental data and demonstrate the usefulness of the models. Additionally, we considered the power handling capability of these devices and describe the various limitations in both conducting and nonconducting states. Our models show that self-aligned gate devices (SAGFET's) have a broad-band cutoff-frequency figure of merit as much as twice that of conventional MESFET's, although the voltage handling capability of the SAGFET is considerably inferior.**

Nomenclature

a^*	Thickness of the channel below the gate metal.
a_{ds}	Depletion region thickness due to the free-surface potential.
a_{dm}	Depletion region thickness due to the metal–semiconductor junction.
C_{nc}	Nonconducting-state total equivalent capacitance.
C_i	Intrinsic capacitance in the conducting state between gate and channel.
C_{igs}	Intrinsic capacitance in the nonconducting state between gate and source.
C_{igd}	Intrinsic capacitance in the nonconducting state between gate and drain.
C_{isd}	Intrinsic source-to-drain capacitance (used for self-aligned-gate devices).
C_{egs}	Extrinsic capacitance in either state between gate and source.
C_{egd}	Extrinsic capacitance in either state between gate and drain.
C_{esd}, C'_{esd}	Extrinsic capacitance in the nonconducting state between drain and source, through the GaAs and through air respectively.
C_{gs}, C_{gd}	Equivalent gate-to-source and gate-to-drain capacitance respectively.
$K(k)$	Complete elliptic integral of the first kind.
F_{cs}	Broad-band cutoff frequency figure of merit.
L_{gd}	Distance between gate metal and drain metal.
L_{gs}	Distance between gate metal and source metal.
L_{sd}	Distance between source metal and drain metal.
L_g	Gate length.
L'_{gd}	For structure B the distance between the drain deep n^+ contact and the edge of the recess depth; for structures A and D the distance between drain n^+ deep contact and the metal gate; and for structure C the distance between drain metal and the edge of the recess.
L'_{gs}	For structure B the distance between source deep n^+ contact and edge of the recess depth; for structures A and D the distance between source n^+ deep contact and metal gate; for structure C the distance between source metal and edge of the recess.
L'_g	Adjusted gate-length L_g to include recess extensions; same as L_g for structures A and D.
L_s, L_d	Length of source and drain metallizations respectively (assumed to be equal).
L'_s, L'_d	Adjusted length of source and drain metallization respectively (see Fig. 2).
q	Electron charge (positive).
R_c	Total conducting-state resistance.
R_{cc}	Contact resistance for metal-to-n^+ interface.
R_{c0}	Contact resistance due to metal-to-n^+ interface and n^+ deep contact layer.
R_{bias}	Resistance in series with the gate.
r_d	Recess depth.
R_p	Conducting-state nonchannel resistance.
R_{p1}	Parasitic resistance with n^+ surface layer (see the Appendix).
R_{ch}	Conducting-state channel resistance.
R_{gd}	Resistance between the drain contact and the channel.
R_{gs}	Resistance between the source contact and the channel.
t_{ds}	Depletion region thickness in the heavily doped surface layer due to the surface potential.
t^*	Surface n^+ layer thickness.
V_p	Magnitude of the applied voltage to pinch-off the channel.
V_{bias}	Magnitude of the dc voltage at the gate.
W	Gate width of the MESFET.
ρ	Resistivity of the channel region.

Manuscript received December 13, 1988; revised August 25, 1989. This work was supported by the Advanced Semiconductor Operations Division of M/A-COM.

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IEEE Log Number 8932006.

0018-9480/90/0200-0109$01.00 ©1990 IEEE

ρ_+ Resistivity of the heavily doped region (assumed to be $2.5 \times 10^{-3}\ \Omega \cdot \text{cm}$).
ϵ_0 Permittivity of free space.
ϵ Permittivity of GaAs.

I. Introduction

During the past few years, considerable work has been done on designing and manufacturing control components using GaAs MESFET devices. This increased interest is attributed to improvements in GaAs processing technology and the attractive features of GaAs MESFET switches (such as low bias power, fast switching speed, MMIC compatibility, and broad-band capabilities). The MESFET used as a passive control device is basically a voltage-controlled resistor whose value is determined by the dc bias voltage applied at the gate of the device. For most control applications, the MESFET is switched between a low-impedance, or conducting, state and a high-impedance, or nonconducting, state, corresponding to the linear and the cutoff regions of the FET characteristics respectively. At frequencies of most interest (below 30 GHz) the conducting state source-to-drain impedance is mostly resistive while in the nonconductive state the impedance is mostly capacitive.

Earlier work has identified the conducting state resistance, R_c, and the nonconducting state capacitance, C_{nc}, as the key equivalent circuit elements used in characterizing broad-band MESFET switches [1], [2]. Based on R_c and C_{nc} the broad-band cutoff frequency figure of merit can be defined as

$$F_{cs} = \frac{1}{2\pi R_c C_{nc}}. \quad (1)$$

In this paper the design considerations for GaAs control MESFET's (particularly for broad-band applications) are evaluated, and future performance capabilities are examined. The paper is organized as presented below.

In Section II, equivalent circuit parameters for the two states of the MESFET control device are developed for the four different device structures shown in Fig. 1. Device structure A is a planar device, B is a gate recessed structure, C is a gate recessed structure with a surface n^+ layer and D is a self-aligned-gate FET (SAGFET). In Section III the power handling capability of MESFET control devices is described. In Section IV a variety of previously reported discrete device characteristics are compared to the modeled parameters. In addition, a dual 2-throw component is evaluated under both low and high power conditions. In Section V, the various device structures are compared.

II. Modeling of Equivalent Circuit Parameters

In this section the resistances and capacitances are modeled from first principles in such a manner that closed-form analytical equations can be derived. Since our focus is mainly on the effect of the geometrical shape of the MESFET on the values of the equivalent circuit elements, we assume uniform doping profiles throughout.

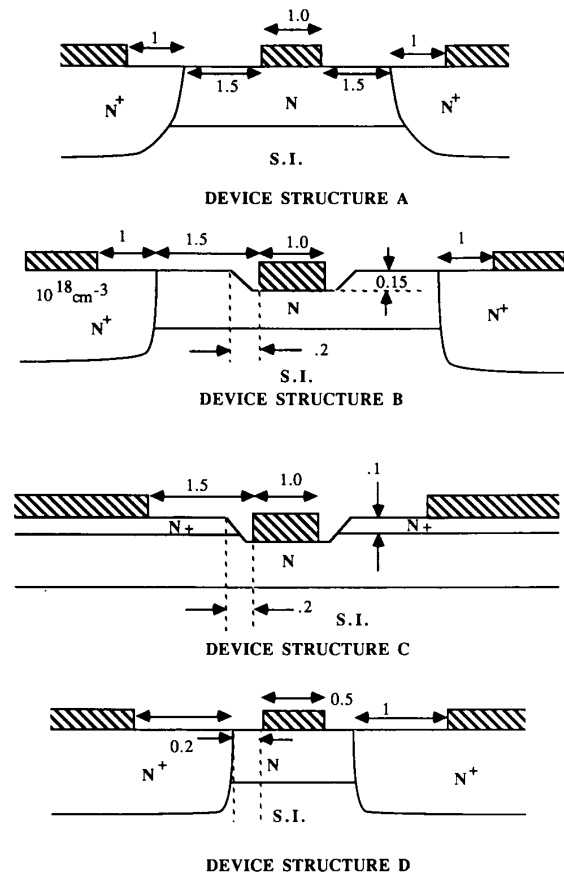

Fig. 1. The MESFET device structures (with typical dimensions). All dimensions are in microns. The N^+ doping is $10^{18}\ \text{cm}^{-3}$.

A. Resistance Modeling

For control applications, the conducting-state resistance of the MESFET device can be subdivided into the channel resistance, R_{ch}, and the parasitic resistance, R_p. The channel resistance must be small in the conducting state, while in the nonconducting state the channel is fully depleted so that the channel resistance is very large and relatively unimportant (capacitive impedances dominate in the nonconducting state).

The parasitic resistance is the combination of the metal-to-semiconductor contact resistance and the resistance of the semiconductor between the contacts and the channel. With recessed gate technology and practical device dimensions, the contact resistance R_{c0} is usually negligible. Thus, we initially neglect any contact resistance and reintroduce this contribution later in considering short gate SAGFET's where the contact resistance becomes important.

The conducting-state resistance of structure A is relatively simple to calculate. Including the surface depletion due to the free-surface pinning voltage and the gate-metal

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