Investigation of Anti-Islanding Protection of Power Converter Based Distributed Generators Using Frequency Domain Analysis

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Abstract—**The anti-islanding algorithm proposed by the Sandia National Laboratories is analyzed in this study because this scheme, also known as the Sandia scheme, is considered to be effective in detecting islanding of distributed generation systems. Previously, other than heuristic approaches, there has not been any quantitative analysis for tuning the control gains of the algorithm based on the power rating and bandwidth of the distributed generation (DG) power converter. The paper interprets the components of the algorithm that affect the voltage magnitude and frequency into block diagrams that can be linearized and studied using continuous time approximations. This paper uses frequency domain approach to analyze the range for the gains required by anti-islanding algorithm to effectively determine the disconnection of the mains grid within an acceptable time duration. The analysis provides guidelines for using the Sandia's schemes under different application conditions. The results are validated using detailed time domain DG and power system simulations.**

Index Terms—**Anti-islanding, distributed generation (DG), inverters, power conditioning, power system protection, power system simulation, power system state estimation, Sandia frequency scheme, Sandia voltage scheme.**

I. INTRODUCTION

ISLANDING of a grid connected distributed generation (DG) occurs when a section of the utility system containing such generators is disconnected from the main utility, but the independent DGs continue to energize the utility lines in the isolated section (termed as an island). Unintended islanding is a concern primarily because it poses a hazard to utility and customer equipment, maintenance personnel, and the general public. Poor power quality can damage loads in the island. Another concern is the out of phase switching of reclosers leading to damage to the DG, neighboring loads, and utility equipment.

Many techniques have been proposed to prevent islanding caused by DGs [1]–[9]. An algorithm proposed by the Sandia National Laboratories is analyzed in this study because it is considered to be effective in detecting the formation of such islands [1], [4]. Sandia's active islanding algorithms had been developed for single-phase inverter units. The algorithm consists of the Sandia frequency shift (SFS) and the Sandia voltage shift (SVS) schemes. The principle behind both the methods is an accelerated frequency and voltage drift created with positive feedback. In the presence of the utility, the frequency and voltage shifts are not effective in drifting the two parameters. However, once the grid is disconnected, these methods force the frequency and/or voltage to shift outside the operating windows, causing the inverter to disconnect due to o/u voltage and frequency protection.

Since these were originally developed for a single-phase inverter, the technique adopted to measure frequency is based on the zero crossing of the voltage waveform, and the voltage magnitude is obtained from RMS calculations. This method has been extended to three phase DGs that utilize three-phase continuous tracking phase locked loop (PLL) in a synchronous reference frame [10].

II. ANALYSIS OF SANDIA ANTI-ISLANDING ALGORITHM

Implementation of the Sandia anti-islanding algorithm is described in [1]. However, a systematic approach to tuning these algorithms has not been described in literature before. The parameters design is mostly performed on a heuristic basis to date.

A block diagram interpretation of the Sandia's algorithm is shown in Fig. 1. This block diagram model of the anti-islanding algorithms is to determine the gain settings for the SVS and the SFS algorithms. The critical gains of the Sandia anti-islanding algorithm are

- K_f for the SFS;
- K_{vp} and K_v for SVS;
- ω_{f1} for the wash out functions;
- ω_{f2} for the real and reactive power regulation loop.

The critical gains for SFS and SVS have to be determined for resistance–inductance–capacitance (RLC) loads (set according to IEEE 1547) so as to mitigate islanding situations [11]. The gain settings of the algorithm, shown in Fig. 1, have been obtained by performing a small signal analysis of the DG system with the tuned RLC load (according to IEEE 929–2000 and UL 1741 anti-islanding test specifications) [12], [13].

The basic principle of the algorithms can be described as follows.

For SVS, the inverter terminal voltage variation can be obtained by the washout function. Then after gains K_v and $P*K_{\mathrm{vp}}$, a power variation is obtained and add onto the original power reference. After divided by the voltage magnitude, the current reference magnitude $\mathrm{Id}*$ is obtained to generate inverter

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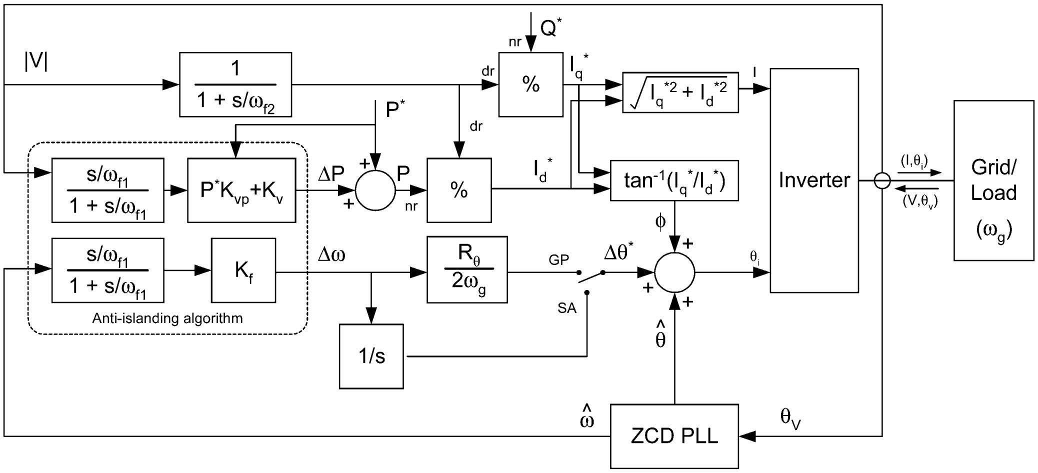

Fig. 1. Block diagram representation of the Sandia's anti-islanding algorithm.

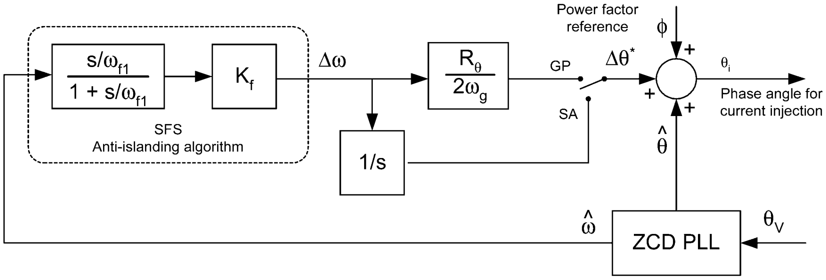

Fig. 2. Block diagram highlighting the SFS component of the Sandia's anti-islanding algorithm.

current magnitude reference. There is a positive feedback loop in that when voltage becomes higher, the current reference will become higher and causes the voltage even higher. Consequently over voltage relay will trip to protect the system from a sustained islanding situation. This loop, however, is only dominantly effective when islanded. When grid connected, the loop has minimal effect on the voltage since the grid is regulating the voltage. A similar control philosophy applies to SFS. The SVS modifies DG power reference based on measured voltage magnitude and the SFS modified current phase angle based on measured frequency. Hence, these schemes act differently compared to traditional power system exciter and governor functions.

The algorithm gains are determined by investigating the open loop behavior as a function of frequency. The voltage magnitude and the phase signal flow paths were opened so as to obtain the SVS and SFS gains, respectively. The Sandia voltage and frequency schemes and the derivation of the block diagram representations are explained in detail as follows.

A. SFS Algorithm

The block diagram of the SFS algorithm is shown in Fig. 2. The frequency estimate from the PLL is passed through a washout function to determine changes in the ambient frequency. This information multiplied by the SFS gain, is added to the frequency reference of the current injected by the DG inverter. As the DG commanded frequency on average cannot be different from the grid frequency, the phase angle has to be periodically reset for meaningful power transfer from the DG to the rest of the grid system to occur. In the single-phase case, this reset of the phase angle in the DG current reference waveform occurs at the voltage zero crossings.

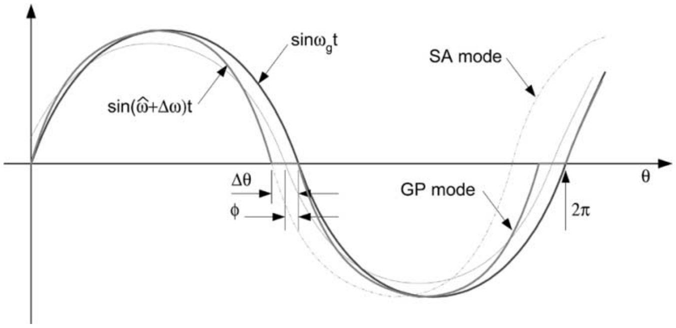

Fig. 3. Nature of waveforms caused by the SFS algorithm.

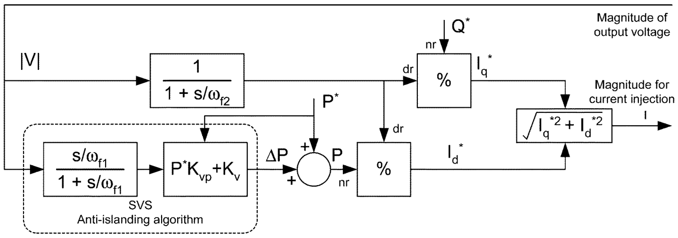

Fig. 4. Block diagram highlighting the SVS component of the Sandia's anti-islanding algorithm.

In grid parallel mode (GP), the grid sets the frequency of operation of the DG. The $R_\theta/2\omega_g$ block in Fig. 2 is an equivalent representation of the actual DG system behavior that captures the change in the phase corresponding to the error in frequency. The derivation of this block in the GP is based on the equivalent phase