Design, Analysis, and Real-Time Testing of a Controller for Multibus Microgrid System

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Abstract—**This paper concentrates on the design and analysis of a controller for multibus microgrid system. The controller proposed for use with each distributed generation (DG) system in the microgrid contains inner voltage and current loops for regulating the three-phase grid-interfacing inverter, and external power control loops for controlling real and reactive power flow and for facilitating power sharing between the paralleled DG systems when a utility fault occurs and the microgrid islands. The controller also incorporates synchronization algorithms for ensuring smooth and safe reconnection of the micro and utility grids when the fault is cleared. With the implementation of the unified controller, the multibus microgrid system is able to switch between islanding and grid-connected modes without disrupting critical loads connected to it. The performance of this unified controller has been verified in simulation using a real-time digital simulator (RTDS[1]) and experimentally using a scaled laboratory prototype.**

Index Terms—**Distributed generation (DG) system, hardware in-the-loop-simulation, microgrid, paralleled operation, power flow control.**

I. INTRODUCTION

IN THE last few years, small distributed generation (DG[2]) systems, typically around 100 kW, have been gaining popularity amongst industry and utilities due to their higher operating efficiencies and lower emission levels. These DG systems are powered by microsources such as fuel cells, photovoltaic cells, batteries, and microturbines etc., and have already been used to share peak generation during peak load hours when energy cost is high and to provide standby generation during system outages [1]. A more recent concept is to group a cluster of loads and paralleled DG systems within a certain local area to form a microgrid [2], [3]. Being a systematic organization of DG systems, a microgrid has larger power capacity and more control flexibilities to fulfill system reliability and power quality requirements, in addition to all the inherited advantages of a single DG system.

Proper operation of the microgrid in both the grid-connected and islanding modes requires the implementation of high performance power flow control and voltage regulation algorithms. The implemented control algorithms should preferably have no communication links between the paralleled DG systems, which can be located far apart. Thus, the control algorithms of each individual DG system should be designed to use only feedback variables that can be measured locally. Other desired performance features include the appropriate sharing of changed power demand in a predetermined manner between the paralleled DG systems when a utility fault occurs and the microgrid islands, and the proper resynchronization of the micro and utility grids for smooth reconnection when the fault is cleared.

To realize the aforementioned performance features, this paper proposes a new unified controller for use with each DG system in the microgrid. By regulating the output voltage, the proposed controller controls power flow in the grid-connected mode of operation, enables real and reactive power sharing between the parallel-operating DG systems when the microgrid islands, and resynchronizes the microgrid with the utility before reconnecting them. The presented controller can respond fast, allowing the controlled microgrid to transit smoothly between the grid-connected and islanding modes without disrupting critical loads connected to it. The performance of the proposed controller has been tested extensively in simulation using a real-time digital simulator (RTDS) and experimentally using a scaled hardware prototype.

II. SYSTEM CONFIGURATION

Fig. 1 shows the multibus microgrid configuration considered in this paper, where two paralleled DG systems 1 and 2 are employed. Each DG system is comprised of a dc source, a pulse-width modulation (PWM) voltage source inverter (VSI) and LC filters. Under normal mode of operation, the microgrid is connected to the utility system at the point of common coupling (PCC) usually through a static transfer switch (STS). In this mode, the two DG systems are controlled to provide local power and voltage support for critical loads 1–3. This configuration reduces the burden of generation and delivery of power directly from the utility grid and enhances the immunity of critical loads to system disturbances in the utility grid.

When a utility fault occurs, the STS opens to isolate the micro and utility grids within half a line frequency cycle. The two DG systems are now the sole power sources left to regulate the load

[1]Built by RTDS Technologies, Inc., Winnipeg, MB, Canada (http://www.rtds.com).

[2]Without specific notification, DG in this paper means small capacity generation units around 100 kW.
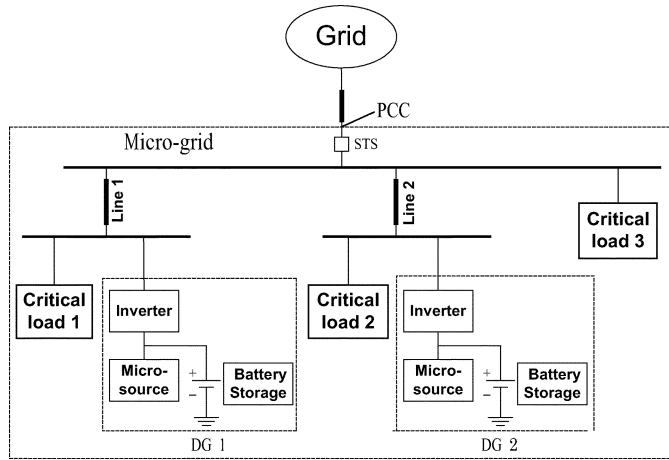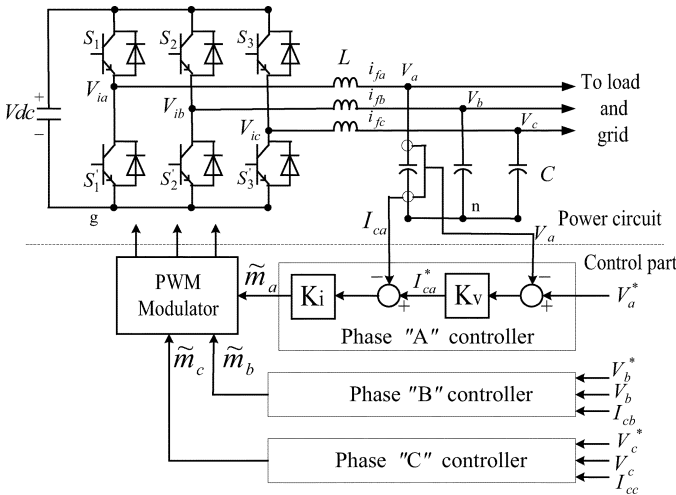
Fig. 1.   Microgrid configuration.

Fig. 2.   Power circuit and control schematic for the three-phase grid-interfacing inverter with LC filters.

voltages and to supply uninterrupted power in a certain prede-termined DG power sharing scheme to all critical loads within the microgrid. Subsequently when the fault is cleared, the mi-crogrid has to be resynchronized with the utility grid before the STS can be reclosed to return the system smoothly back to the grid-connected mode of operation.

III. CONTROLLER DESIGN

This section presents the design of a unified controller for use with each DG system to allow the microgrid in Fig. 1 to function as described in Section II. (The proposed controller can also be used for more complex microgrids where more DG systems operate in parallel, even though a microgrid with only two DG systems is considered in this paper for illustration).

A. Inner Voltage and Current Control Loops

The inner current-regulated voltage-controlled strategy used for controlling the three-phase grid-interfacing VSI is shown in Fig. 2 [4], [5]. As shown, an outer capacitor voltage feedback compensator K_v is used to force the capacitor voltages $\{V_a, V_b, V_c\}$ to track their sinusoidal reference wave-forms $\{V_a^*, V_b^*, V_c^*\}$ stiffly with an acceptable low output

total harmonic distortion (THD). The outputs of this voltage compensator $\{I_{Ca}^*, I_{Cb}^*, I_{Cc}^*\}$ are then fed to an inner capacitor current compensator K_i, acting as the capacitor current refer-ence signals for this inner compensator. The inner capacitor current compensator is included here mainly to stabilize the system and to improve the system dynamic response by rapidly compensating for near-future variations in the load voltages whose rate of change is indirectly sensed by measuring the ca-pacitor currents. The output modulating signals $\{\widetilde{m}_a, \widetilde{m}_b, \widetilde{m}_c\}$ from the inner current compensator are finally fed to the sinusoidal pulse-width modulator (SPWM) to generate the high frequency gating signals for driving the three-phase VSI.

To allow for transfer function analysis of the control scheme shown in Fig. 2, the single-phase equivalent model of the grid-interfacing inverter is first derived, as

$$L\frac{di_{\text{fa}}}{dt} = S_1^* V_{\text{dc}} - (V_{\text{an}} + V_{\text{ng}}) \tag{1}$$

$$L\frac{di_{\text{fb}}}{dt} = S_2^* V_{\text{dc}} - (V_{\text{bn}} + V_{\text{ng}}) \tag{2}$$

$$L\frac{di_{\text{fc}}}{dt} = S_3^* V_{\text{dc}} - (V_{\text{cn}} + V_{\text{ng}}) \tag{3}$$

where S_j^* represents the state of each semiconductor switch ($S_j^* = 1$ when switch S_j is ON and $S_j^* = 0$ when switch S_j^* is ON, $j = 1, 2,$ or 3), V_{dc} is the dc-link voltage, V_{xn} is the phase to neutral voltage, and i_{fx} is the current through filter inductor L. ($x = a, b,$ or c).

Assuming that the three-phase loads and grid voltages are balanced, then

$$V_{\text{an}} + V_{\text{bn}} + V_{\text{cn}} = 0 \tag{4}$$

$$i_{\text{fa}} + i_{\text{fb}} + i_{\text{fc}} = 0. \tag{5}$$

Substituting (4) and (5) into the sum of (1)–(3), V_{ng} can be expressed in terms of the switch states as

$$V_{\text{ng}} = \frac{V_{\text{dc}}}{3}\left(S_1^* + S_2^* + S_3^*\right). \tag{6}$$

For a high "switching to modulating frequency" ratio, the dis-crete variable S_j^* can be replaced by its duty cycle expressed as

$$d_j = \frac{m}{2}\cos\left[\omega t - \varphi - (j-1)\frac{2\pi}{3}\right] + \frac{1}{2} \tag{7}$$

where φ is the phase shift and m is the modulation index. Re-placing S_j^* by d_j, (6) can be simplified as $V_{\text{ng}} = V_{\text{dc}}/2$. Equa-tions (1)–(3) can then be re-expressed as

$$L\frac{di_{\text{fa}}}{dt} = \frac{1}{2}m\cos(\omega t - \varphi)V_{\text{dc}} - V_{\text{an}} \tag{8}$$

$$L\frac{di_{\text{fb}}}{dt} = \frac{1}{2}m\cos\left(\omega t - \varphi - \frac{2\pi}{3}\right)V_{\text{dc}} - V_{\text{bn}} \tag{9}$$

$$L\frac{di_{\text{fc}}}{dt} = \frac{1}{2}m\cos\left(\omega t - \varphi + \frac{2\pi}{3}\right)V_{\text{dc}} - V_{\text{cn}} \tag{10}$$

and the final governing differential equations for each phase (with no intercoupling between phases) can be written as

$$L\frac{dI_f}{dt} = \frac{1}{2}\widetilde{m}V_{\text{dc}} - V_C \tag{11}$$