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Reduction of Transmission Line Losses Using VLSI Interconnect

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Abstract

60-70% of the power generated is lost during transmission and distribution phase. Out of this maximum losses occur at transmission and distribution line interconnects, which comprises 40 to 50% of the total loss. To reduce this scientist have come up with an idea of using VLSI interconnects. We analyzed various methods of R-L-C interconnect used currently and losses that take place due to them. Further in our study CMOS interconnects were implemented in the same circuit and their results were analyzed. Traditionally, the total delay (i.e., latency) of a circuit is considered to measure its performance. The total delay comprises of two components, the transistor delay and the interconnect delay. Interconnect delay, which was once considered to be quite insignificant has become a major problem with the growing worldwide network. While trying to find economical, practically feasible and implementable method for reduction of transmission line losses, we did real time simulation of various combinations of CMOS circuit of a transmission line model and studied its characteristic. The variation in characteristic with respect to time gave a preview of effect of change of various configuration of passive element with CMOS design circuit. The effect of crosstalk was also analyzed.

Keyword: *Interconnect Dela; transmission line lose; R-L-C parameter; power reduction..*

Introduction:-

With the scaling of CMOS technology, the global interconnect delay that was once significantly smaller than the transistor delay has now become a few hundred times larger than the transistor delay As a result, on-chip interconnects are limiting the maximum performance that can be achieved on processor systems

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With the help of models and methodologies we can develop the design rules to optimize performance, power, and area of VLSI global interconnect networks through a simultaneous application of voltage scaling and wire sizing. By qualitative analysis of latency, throughput, signal integrity, power dissipation, and area we can compares the results of design optimizations to those of conventional global interconnect circuits.
With Transistors and interconnects, the next-generation billion-transistor Itanium microprocessor has set out to achieve an industry-leading performance of 1 GHz. Interestingly, the processing power has moved from performing simple calculations to managing complex billion-transistor systems in a relatively short period of time. With the Current available technology the interconnect problem has a long way to go. Constructive fabric combined with architectural and system-level solution has to be developed. Earlier we used programmable Interconnect, but it had substantial cost in performance and power, in performance in area and we faced the problem of power dissipation
Capacitive crosstalk in dense wire network affects the reliability of the system and therefore its performance [1]. Careful design using well-behaved regular structure or using advance design automation tool is a necessity. Providing the necessary shielding is important for wire such as busses or clock signals. Driving large capacitance rapidly in CMOS requires introduction of a cascade of buffer stage that must be carefully sized. More advance techniques include the lowering of single swing on long wires, and the use of current mode signaling. Resistivity affects the reliability of a circuit by introducing IR drops. This is especially important for supply network, where wire sizing is important.
The exact delay introduced by the RC effects can be minimized by repeater insertion and by using a better interconnect technology. The Inductance of interconnect becomes important at higher switching speed. The chip package is currently one of the most important contributors of inductance. Novel packaging techniques are gaining importance with fast technologies. Ground bounce introduced by the L di/dt voltage drop over the supply wire is one of the most important sources of noise in current ICs. Ground bounce can be reduced by providing sufficient pins and by controlling the slope of the off-chip signals. Transmission-line effects are rapidly becoming an issue in super GHz design. Providing the correct termination is the only of dealing with transmission delay.

Determining and quantifying interconnect parameter:-

Wiring of today's IC's form a complex geometry that introduces capacitive, resistive, and inductive parasitic They all cause an increase in propagation delay, introduce noise and have impact on energy dissipation and power distribution which impact the reliability of the circuit.

Introducing circuit models for interconnect wires:-

The designer of electronic circuit has multiple choices in realizing interconnection between various devices that make up the circuit. State of art process offer multiple layer of aluminium or copper, and at-least one layer of poly-silicon. Heavily doped n+ or p+ is also used for wiring which makes the complex geometrical structure of integrated circuit used today that introduces parasitic capacitance, inductance and resistance. All these have multiple effects on circuit behaviour:-

- They all cause an increase in propagation delay, hence drop in circuit performance.
- They all have an impact on energy dissipation and power distribution
- They all cause the introduction of extra noise sources, which affect the reliability of the circuit.

This design is totally useless in today's IC design. As many problem are observed with real time design. Inductive effects can be ignored if resistance of wire is substantial enough, this is the case for long Aluminum wires with a small cross section, or if the rise and fall times of applied signals are slow. When the wire are short, the cross section of the wire is large, or the