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Low cost and highly reliable radiation hardened latch design in 65 nm CMOS technology ☆

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ABSTRACT

As a consequence of technology scaling down, gate capacitances and stored charge in sensitive nodes are decreasing rapidly, which makes CMOS circuits more vulnerable to radiation induced soft errors. In this paper, a low cost and highly reliable radiation hardened latch is proposed using 65 nm CMOS commercial technology. The proposed latch can fully tolerate the single event upset (SEU) when particles strike on any one of its single node. Furthermore, it can efficiently mask the input single event transient (SET). A set of HSPICE post-layout simulations are done to evaluate the proposed latch circuit and previous latch circuits designed in the literatures, and the comparison results among the latches of type 4 show that the proposed latch reduces at least 39% power consumption and 67.6% power delay product. Moreover, the proposed latch has a second lowest area overhead and a comparable ability of the single event multiple upsets (SEMUs) tolerance among the latches of type 4. Finally, the impacts of process, supply voltage and temperature variations on our proposed latch and previous latches are investigated.

1. Introduction

With the technology scaling down, circuits have become more and more sensitive to radiation, which make the reliability issue of circuits become one of the major concerns for circuit designers [1]. Due to the reduction of supply voltage and node capacitance, the amount of charges that can be stored on a node is also reduced, making the circuit susceptible to particle-induced charge. When the amount of accumulated particle-induced charge is high enough, a transient fault will appear as an electrical pulse which is called a single event transient (SET). In addition, the current induced by a particle hit always flows from n-type diffusion to p-type diffusion through a p–n junction [2,3]. It means that if a latch is made up of only PMOS transistors, a radiation particle strike cannot flip the node voltage from 1 to 0; vice versa, if only NMOS transistors, the node voltage cannot flip from 0 to 1 [4]. If an SET propagates through the combinational logic circuits and once be latched by the downstream sequential logic cell such as memory cell or latch, a single event upset (SEU) will happen, which causes the stored value to be incorrectly flipped in memory cell or latch. For memory cells, error correction codes (ECC) [5–9] can be used at low cost to tolerate SEUs due to particle strike. However, latches are integrated into the logic and widely spread across the chip, ECC cannot be employed [10].

Researchers devote to harden latches by adding additional transistors to its basic circuit structure, and many radiation harden latches have been proposed [11–18]. We can classify these latches (will be discussed in details in Section 2) into four different types similar to [12,18]. The first type (type 1) of latches are those that they have more capability of tolerating SEU than traditional latches, but they are not fully SEU immune. In other words, these latches have one or more nodes to which an energetic particle strikes, could corrupt their latched value. The latches designed in [11,12] are of type 1. The second type (type 2) of latches are those that they can fully tolerate SEU when particles strike on any one of its single node, but they cannot filter out the input SET and its output node will take a high impedance state when a particle strikes on some of their internal single node. The latches designed in [13, 14, HLR, 15] are of type 2. Type 3 latches are those ones that they are fully SEU immune when particles strike on any one of their single node and their output nodes will not take high impedance states, but they cannot filter out the input SET. The proposed latches in [14, HLR-CG1 and HLR-CG2, 16, 17, FERST] are of type 3. Type 4 latches are those ones that they are fully SEU immune when particles strike on any one of their single node and the output nodes will not take high impedance states; they can filter out the input SET,

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too. The proposed latches in [17, Enhanced version of FERST mentioned as EVFERST here, 18] are of type 4.

In this paper, we propose a low cost and highly reliable radiation hardened latch which is belong to the category of type 4. Simulation results are carried out by means of HSPICE with 65 nm CMOS commercial technology. Compared with previous type 4 latches, the proposed latch has a much better performance in terms of power, D to Q delay and power delay product (PDP), and has a second lowest area overhead as well as a comparable ability of single even multiple upsets (SEMUs) tolerance. The impacts of process, supply voltage and temperature variations on proposed latch are also analyzed.

The remaining of this paper is organized as follows: Section 2 gives a review of previous hardened latch designs. In Section 3, the proposed low cost and highly reliable hardened latch is discussed. Simulation results of both the proposed latch and previous latches are shown in Section 4. Section 5 investigates the impact of process, supply voltage and temperature variations on the proposed latch. Section 6 concludes this paper.

2. Previous works

The latches designed in [11,12] are of type 1. As shown in Figs. 1 and 2, both latches are based on the hysteresis property of Schmitt trigger circuit (S) and time redundancy to tolerate SET. The latches in [11,12] are more reliable than traditional latches, but as mentioned in Section 1, they are not fully immune. For example, the latch designed in [11] may upset when an energetic particle strikes on its node int1 or even strikes on its output node Q, while the latch designed in [12] may also upset when an energetic particle strikes on its node nq.

In order to solve the problems mentioned in type 1 latches, the latch designed in [13], belonging to type 2, has been proposed and is shown in Fig. 3. Compared with type 1 latches, the latch designed in [13] can guarantee not to be affected by any single node particle strike, but it does not have the ability of input SET filtering. Besides, if an energetic particle strikes on its node int5 (or int6), nodes int1 and int2 (or int3 and int4) may both upset, making int5 (or int6) a permanent flip. Then the value stored on node int5 becomes opposite to the value stored on node int6 which results in a high impedance state on output node Q. Further improvements have been made in type 3 latches [14, HLR-CG1 and HLR-CG2, 16, 17, FERST]. They can tolerate any single node particle strike and can prevent the output nodes from taking high impedance states. However, they cannot filter out input SET.

To solve above problems, three robust latch structures have been designed in [17, EVFERST, 18], which are of type 4, shown in Figs. 4 and 5. Those latches are the most reliable latches due to their toleration of any single node particle strikes and ability to filter out input SET, as well as the feature to not take a high impedance state at output node. However, the latch designed in [17, EVFERST] has a massive amount of transistors resulting in high power consumption and large area; latches proposed in [18] have active feedback loops when they work at their transparent modes, which also lead to high power consumptions.

In addition, all the latches discussed above suffer from the problem of having active feedback loop to some extent when work at their transparent modes, which would increase power consumptions. This problem will be properly solved by our proposed latch which is of type 4, shown in Section 3.

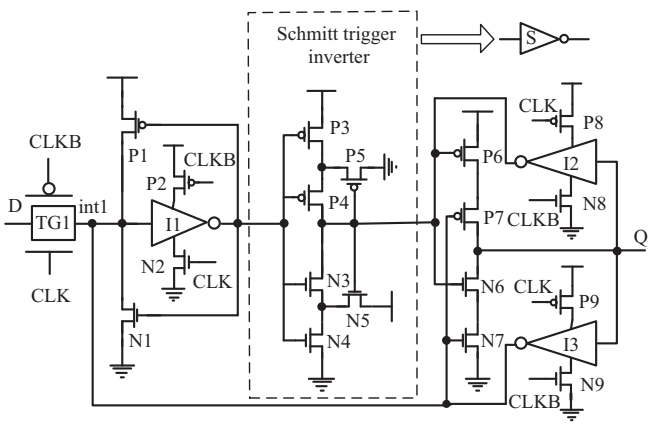

Fig. 1. Hardened latch proposed in [11].

3. Proposed hardened latch design

The proposed latch shown in Fig. 6 overcomes the defects mentioned in Section 2 by reasonable structure design, which allows designers to cut off all the loops when works at its transparent mode. By using clocked inverters in all feedback loops and clocked C-element, power consumption is reduced. Besides, the proposed latch can reuse its part3 to attain the capability of SET tolerance and prevent the output node from taking its high impedance state. While, the functions of tolerating SET and preventing high impedance state are implemented by two parts in LSEH-1 latch, this means C-element in LSEH-1 latch has to work actively all the time, which would increases power consumption.

In this proposed latch structure, the input node D is separated into three nodes, which form three paths. Two of these paths are finally applied to the input nodes of C-element through part1 and part2, separately; another one is finally applied to the output node Q of C-element through part3. In this way, when CLK signal takes its one value, the transmission gates TG1, TG2 and TG3 are turned on and the latch works at its transparent mode. D propagates to Q through Schmitt trigger circuit (S), internal node int1 and int4 are connected to node D through TG1 and TG3, respectively. Internal node int3 is driven by node D through TG2 and inverter I3 in order. The inverters I2, I5, I6 and C-element are turned off by the clock signal, in other words, all feedback loops are cut off, including C-element. If the input contains an SET in its transparent mode, the SET pulse will be filtered out due to the hysteresis property of Schmitt trigger circuit (S).

When the CLK signal takes its zero value, the transmission gates TG1, TG2 and TG3 are turned off, the inverters I2, I5, I6 and C-element are turned on, which makes each feedback loop actively and C-element work normally, the latch works at its hold mode. Then, part3 is isolated from input node D, while it is still connected to the output node Q, this can prevent the output node from taking a high impedance state when particles strike on any one of its internal node. That is to say, the part3 can not only filter out input SET in its transparent mode, but also guarantee the output node Q not to take a high impedance state in its hold mode. Therefore, the proposed latch fulfills the reuse of part3.

In the hold mode, the three keepers of part1, part2 and part3, hold the latched value. If node int1 (or int2) is affected by an energetic SET, part1 will upset due to its positive feedback structure, however, this error cannot propagate through the C-element because part2 holds their original values, in other words, the output node Q will not be affected and not be a high impedance state because of part 3; in the same way, if the node int4 (or int5) is affected by the strike of an energetic SET, the output node Q will not be affected, either; if node Int3 is affected by SET, because of the hysteresis property of Schmitt trigger circuit (S), output can hardly be affected, even if output node Q is flipped directly by an energetic SET or indirectly by int3, the output node Q will be