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Visible and NIR integrated Phototransistors in CMOS technology

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ABSTRACT

In this paper we present several different types of fully integrated pnp phototransistors realized in a 0.6 μm OPTO ASIC CMOS process using low doped epitaxial starting wafers. Different types of phototransistors were realized by varying base doping profile and emitter area. This variations lead to different characteristics of the phototransistors. Devices with high responsivities or high bandwidths are achieved. Responsivities up to 98 A/W and 37.2 A/W for modulated light at 330 kHz were achieved at 675 nm and 850 nm wavelengths, respectively. On the other hand bandwidths up to 9.7 MHz and 14 MHz for 675 nm and 850 nm wavelength, respectively, were achieved at the expense of a reduced responsivity. Due to the fact that the used process is a standard silicon CMOS technology, low-cost integration to an integrated optoelectronic circuit is possible. This could lead to possible applications like low-cost, highly sensitive optical receivers, optical sensors, systems-on-a-chip for optical distance measurement or combined to an array even in a 3D camera.

1. Introduction

Photodetectors are used to convert optical into electrical signals. Most used photodetectors are PN-photodiodes, PIN-photodiodes, avalanche photodiodes (APD) and phototransistors (PT). The goal of the PTs as well as APDs is to increase the responsivity compared to conventional photodiodes. For integrated circuits, different types of photodetectors can be built in a standard CMOS process.

Photodiodes can be realized for high speed or high responsivity applications. The characteristics of detectors depend strongly on the used wavelength. Near infrared (IR) light, e.g. 850 nm, has a 1/e penetration depth of around 16 μm whereas red light, e.g. 675 nm, has a penetration depth of 4.1 μm in silicon [1]. The PN-photodiode consists of a basic p–n junction, which can be realized by two different layouts in a standard CMOS process. Each structure has advantages in either high speed or high responsivity.

First, a PN diode can be realized by an n-well/p-substrate diode. This structure can receive photons of the complete visible and near infrared spectrum. The large penetration depth of the near infrared light leads to long travel distances for charges in the field free diffusion region. Therefore this structure has a large diffusion and a small drift current portion for near-infrared light. This leads to a slow detector.

Second, a PN diode can be built by a p+/n-well structure, which is inherently isolated in a common p-substrate. The photosensitive structure will be only around 1 μm thick and every electron–hole-pair generated by photons in the substrate will be lost for the photodiode. By losing all generated charges deep in the substrate, a main portion of the diffusion current is omitted. Because of this mechanism such structures show a high bandwidth together with a rather low responsivity.

To achieve high bandwidths without losing the deep-generated charges, an additional low doped intrinsic layer is placed in the p–n junction. PN diodes with an additional intrinsic layer are called PIN diodes. For the integration of PIN diodes in a CMOS process, a special starting material is used. This starting material has a 10–15 μm low doped epitaxially grown layer on top of the high doped substrate. The intrinsic zone of the PIN diode is formed by this low doped epitaxial layer. Due to the low doping concentration of the intrinsic layer the extension of the space-charge region (SCR) inside the diode is increased. Therefore charges generated deep in the substrate are now accelerated by the electric field in the thick drift zone. The photodetector becomes faster and shows a rather high responsivity for a photodiode. These characteristics are also the reason why PIN diodes are mostly used as photodetectors for high speed applications, e.g. [2]. Furthermore PIN photodiodes are also used in distance measurement applications as single pixel [3], as line sensor [4] or as 3D camera [5]. Nevertheless, the responsivity of this photodetector is limited under best circumstances to 0.65 A/W and 0.55 A/W for 850 nm and 675 nm, respectively [1].

Photodiodes do not have an internal amplification. Their maximum possible quantum efficiency is 1. Maximum quantum efficiency will occur when all charges generated by photons contribute to the photocurrent. Phototransistors and avalanche photodiodes exceed this limitation with an internal amplification of the primary photocurrent. This amplification is desirable and important for detecting weak optical signals. APDs achieve their amplification by the avalanche multiplication process. This takes

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place at high electric field strengths and needs voltages of at least several tens of volts [6]. Such high voltages are hard to handle in integrated circuits. Furthermore APDs show a very narrow bias voltage range for linear operation and therefore nonlinear behaviour is expected for any changes of the bias voltage. Background light is also amplified in APDs, which can lead to saturation of pixel circuits. This is also the reason why APDs are not practicable for the use in image sensors or distance measurement setups, especially in bright sunlight. Nevertheless there are many other application fields for APDs. Complex bias voltage control circuits are necessary to handle the above mentioned problems in APDs. In Ref. [7] a shallow APD for 430 nm light with a responsivity of 4.6 A/W at a reverse bias of 19.5 V is reported in CMOS. For red and infrared light, the detection probability decreases and much lower responsivities result.

Opposed to APDs PTs do not need such high voltages for their internal amplification. This is the most important advantage of PTs. In a phototransistor a large photodiode is formed by the base-collector diode. Also the base-emitter diode forms a photodiode but usually the area is small and the contribution is negligible. The internal bipolar transistor amplifies the primary photocurrent. Charges generated in the base-collector diode are separated and swept into base and collector. For pnp phototransistors, as shown in Fig. 1, electrons are swept into the base and holes into the collector area. The electron accumulation in the base area makes the potential of the base more negative. This effect leads furthermore to the injection of holes from the p+ emitter into the base. This mechanism amplifies the generated primary photocurrent from the base-collector photodiode. A typical value for the responsivity of a PT in standard-burried-collector (SBC) bipolar or BiCMOS technology at 850 nm presented in [8] is 2.7 A/W. The SiGe PT in [8] has a thin thickness of the base-collector space-charge region of only about 1 μm, which leads to the low responsivity.

In this work we present silicon integrated PTs in a CMOS process with different layouts of the base and emitter area. The presented PTs achieve much higher responsivities than published bipolar SBC PTs. The higher responsivity is achieved due to implementing a deep intrinsic layer for a thick base-collector SCR. Different designs of the base and emitter area can be used to optimize the devices for different goals such as high responsivity or high speed. Cheap CMOS integration of PTs paves the way for optoelectronic integrated circuits (OEICs) and system-on-chip (SoC) with several advantages. Such advantages are e.g. smaller area due to only one die instead of two (one for the photodetector and one for the circuit), no bond wires, handling, packaging and many more advantages. The fact that PTs need only low voltages compared to APDs and show a high responsivity due to the current amplification makes them well suited for different SoC applications like active pixels, light barriers or optocouplers.

2. Device structure options

Several versions of pnp-type PTs with a photosensitive area of $100 \times 100\ \mu m^2$ were implemented in a 0.6 μm OPTO ASIC CMOS process. The only difference to a standard CMOS ASIC process is the use of a special starting wafer for the implementation of the PTs. This special wafer has a thick (~15 μm), low-doped ($2 \times 10^{13}\ cm^{-3}$) p-epitaxial layer and on top a shallow (~1 μm), low-doped ($10^{14}\ cm^{-3}$) n-epitaxial layer. Below is the highly doped p-substrate material. The p-epitaxial layer leads to a PIN structure for the base-collector junction. Thus the device gets a thick SCR even for low voltages. A thick SCR is well suited for light with a high penetration depth, e.g. light with a wavelength of 850 nm. Nevertheless, the bandwidth of PTs is lower than the bandwidth of PIN photodiodes. The reason for this limitation is the fact that PTs have two p–n junctions and thus two capacitances (base-collector capacitance C_{BC} and base-emitter capacitance C_{BE}). An additional bandwidth limiting factor is the base transit time τ_B which is not present in a PD. The definition of the −3 dB bandwidth of a PT is shown in the following equation [9]:

$$f_{-3dB} = \frac{1}{2\pi\beta \cdot \left(\tau_B + \frac{k_B T}{q I_E}(C_{BE} C_{BC})\right)} \quad (1)$$

In (1) β is the current gain, τ_B is the base transit time, k_B is the Boltzmann constant, T is absolute temperature, q is the elementary charge and I_E is the emitter current of the transistor. All PTs have different layout structures. The different structures lead to different characteristics of each device. The following subsections describe the collector (p-substrate), base (n-region) and emitter (p-region) areas.

2.1. Collector area

The collector is formed by the p-type substrate. It is connected via a large-area ring of substrate contacts on the border of the PT and tied to substrate potential. Due to this fact the PT can only be used in emitter follower setup.

2.2. Base area

A shallow low-doped n-epitaxial layer forms the base. Inspired by Marchlewski et al. [10], the doping concentration of the base can be varied by additional n-well implantations inside the n-epi layer. In this work three different base layouts (Fig. 2) are used.

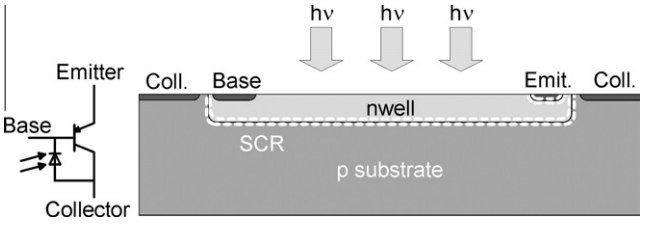

Fig. 1. Schematic and cross section of a phototransistor integrated in a standard CMOS process.

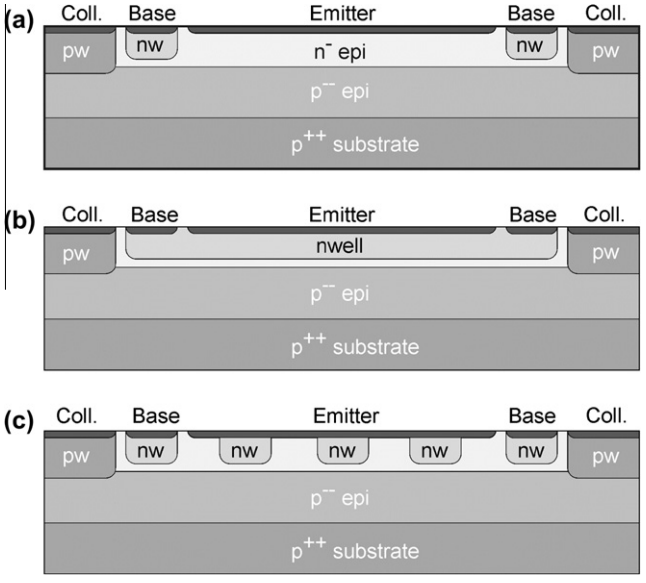

Fig. 2. Different base designs (cross section): (a) base without additional n-doping, (b) base with highest doping concentration, and (c) base with varied doping concentration.