Microelectronics Journal 45 (2014) 1556–1565

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

A new asymmetric 6T SRAM cell with a write assist technique in 65 nm CMOS technology

Hooman Farkhani [a], Ali Peiravi [a], Farshad Moradi [b,*]

[a] Department of Electrical Engineering, Ferdowsi University of Mashhad, Mashhad, Iran
[b] Integrated Circuits and Electronics Laboratory (ICE-LAB), Department of Engineering, Aarhus University, Denmark

ARTICLE INFO

Article history:
Received 26 January 2014
Received in revised form
20 August 2014
Accepted 11 September 2014
Available online 11 October 2014

Keywords:
SRAM
Write Margin
Read Static Noise Margin
CMOS

ABSTRACT

A new asymmetric 6T-SRAM cell design is presented for low-voltage low-power operation under process variations. The write margin of the proposed cell is improved by the use of a new write-assist technique. Simulation results in 65 nm technology show that the proposed cell achieves the same RSNM as the asymmetric 5T-SRAM cell and 77% higher RSNM than the standard 6T-SRAM cell while it is able to perform write operation without any write assist at $V_{DD}=1$ V. Monte Carlo simulations for an 8 Kb SRAM (256×32) array indicate that the scalability of operating supply voltage of the proposed cell can be improved by 10% and 21% compared to asymmetric 5T- and standard 6T-SRAM cells; 21% and 53% lower leakage power consumption, respectively. The proposed 6T-SRAM cell design achieves 9% and 19% lower cell area overhead compared with asymmetric 5T- and standard 6T-SRAM cells, respectively. Considering the area overhead for the write assist, replica column and the replica column driver of 2.6%, the overall area reduction in die area is 6.3% and 16.3% as compared with array designs with asymmetric 5T- and standard 6T-SRAM cells.

1. Introduction

CMOS technology has been the cornerstone of semiconductor devices for years. Moore's law predicts technology down scaling that leads to improvements in performance features such as speed, power consumption and area. Although circuits and systems benefit from technology down scaling in some aspects, the undesired features such as short channel effects (SCEs) and sensitivity to process variations are also consequential. The effect of process variations on performance is a key issue in scaled CMOS technology. This effect gets more pronounced as the size of transistors is reduced. One of the highly sensitive circuits to process variations is SRAM that is due to the use of small devices in order to achieve a higher density. Process variations can be due to global or local mismatches between devices. Global variation refers to die-to-die variations in devices and local mismatch refers to mismatch between transistors on the same die [1]. Local mismatch in SRAM devices can easily lead to read stability degradation (stored data is flipped during read), read failure (data is not read during read period), writeability decrease or write time increase. Besides, improving the write features of the SRAM leads to degradation in its read performance and vice versa.

Fig. 1 shows the standard 6T-SRAM cell structure. It consists of two back to back inverters (PUL–PDL and PUR–PDR) which keep the data and its inverse on nodes Q and QB, respectively. The access transistors (ACL–ACR) are used to perform read and write operations. Due to using a common path (ACL–ACR) for read and write, improving read stability will lead to degradation of writeability of the cell and vice versa. To improve the Read Static Noise Margin (RSNM) of an SRAM cell, beta ratio ($\beta=W_{PD}/W_{AC}$) can be increased, while a lower alpha ratio ($\alpha=W_{PU}/W_{AC}$) is desirable to improve the cell writeability. Finally, during hold mode, equal strength for pull up and pull down transistors sets the trip point of the two back-to-back inverters at $V_{SUPPLY}/2$ and ensures maximum noise margin.

Several solutions have been proposed in the literature from device to architecture levels to improve SRAM cell functionality. For instance, at device level, using new devices such as FinFETs leads to significant SRAM performance improvement [1–4]. At cell level, new cells such as 7T, 8T, 9T, 10T, and 11T [5–11] have been proposed that come with a penalty in area overhead while other proposed cells such as asymmetric 6T and 5T topologies [12,13] occupy the same area compared to the standard symmetric 6T SRAM cell. At architecture level, read and write assist techniques improve SRAM robustness and performance while they occupy

* Corresponding author.
E-mail addresses: Farkhani.hooman@stu.um.ac.ir (H. Farkhani), Peiravi@um.ac.ir (A. Peiravi), moradi@eng.au.dk (F. Moradi).

http://dx.doi.org/10.1016/j.mejo.2014.09.006
0026-2692/

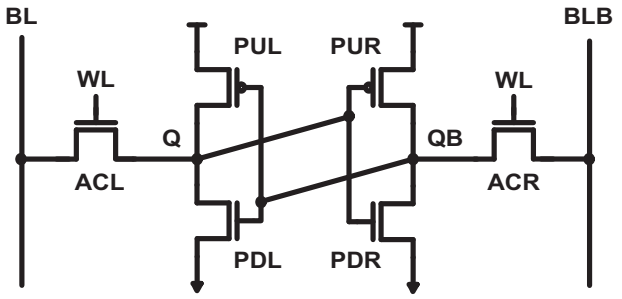

Fig. 1. The standard 6T-SRAM cell.

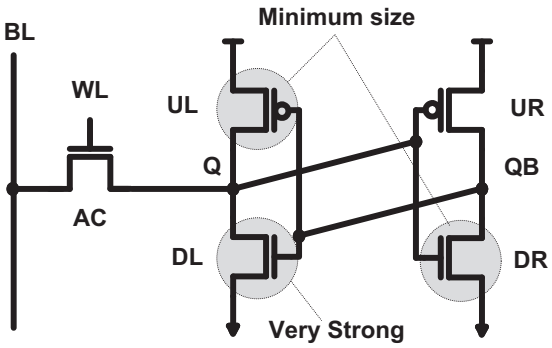

Fig. 2. The asymmetric 5T-SRAM cell [12].

less area in comparison with the cell techniques (e.g. 8T and 10T) and can be utilized with any SRAM cell [14–23].

Memories take up 80% of the die area in high performance processors [24]. Hence, there is a crucial need for a low-leakage, high density, and highly robust SRAM design. Amongst different cell topologies, the asymmetric 5T-SRAM cell is one of the best candidates in order to achieve high density. However, the write margin of the 5T-SRAM cell degrades drastically and this limits the lowering of the supply voltage. This in turn restricts the improvement of the cell leakage power.

In this paper, a new asymmetric 6T-SRAM cell is proposed which can significantly improve read and write performance with less area. The asymmetric 6T-SRAM cell has the advantage of using transmission gate as access device which improves the writeability of the cell. In addition, applying a write assist technique improves the robustness of the cell. It allows SRAM to work at lower supply voltages and this leads to lower leakage power consumption.

Moreover, a new write assist technique that improves the write margin of the proposed 6T-SRAM cell is proposed. The proposed write assist technique applies a boosted voltage ($V_{DD}+\Delta V$) to the bitline during write '1' on the cell. This technique results in significant improvement in the Write Margin (WM) and the Write Time (WT). In this technique, coupling capacitances are used to produce boosted voltages.

The remainder of the paper is organized as follows. In Section 2, a brief survey of existing asymmetric SRAM cells is presented. In Section 3, the basic concept of the proposed asymmetric cell and the proposed boosted bitline (BBL) technique is presented and validated by mathematical analysis. The efficacy of the BBL technique on the proposed 6T-SRAM cell is shown in Section 4 through simulations. Finally, conclusions are drawn in Section 5.

2. State of the art

In this section, the existing asymmetric SRAM cell and the write assist techniques which can improve its inability to write '1' are discussed.

2.1. Asymmetric SRAM cell

Asymmetric SRAM topologies use asymmetric sizing of the cross-coupled inverters to increase RSNM of the standard 6T-SRAM cell with the same size at the cost of WM reduction during write '1' on the cell. Considering the fact that RSNM limits the SRAM operation at lower supply voltages, the RSNM improvement allows scaling down the operating supply voltage. Decreasing the minimum supply voltage together with single-ended access in asymmetric SRAM cells reduces the leakage power consumption. The asymmetric 5T-SRAM cell in [12] is shown in Fig. 2. Two different sizing scenarios used in [12] shown in Fig. 2 are 1) maximum RSNM (RSNM Max) and 2) maximum WM (WM Max). In this cell, asymmetric sizing is used for the cross-coupled inverters. The strong pull down transistor (DL) connected to the access transistor decreases the increment in the voltage of storage node (V_Q) during read. Moreover, using minimum size pull down transistor (DR) in the inverter with its input connected to Q (right hand) increases its trip point. The above changes including the lower increase in V_Q and higher trip point in the right hand inverter significantly improve RSNM of the asymmetric 5T-SRAM cell. The main drawback of the asymmetric SRAM cell during write mode is when writing '1' without any write assist. This is attributed to the strong pull down transistor and the very large bitline capacitance.

2.2. Write assist techniques

In order to improve write margin of SRAMs, several write assist techniques have been proposed. Some of these techniques rely on cell V_{DD} collapse [14–17], Negative Bit-Line (NBL) [18–22], Boosted Word-Line (BWL) and cell GND boost [23]. Amongst the existing proposed techniques, NBL write assist is the most effective one to reduce SRAM minimum supply voltage, especially when considering dynamic failure metrics [25]. This technique improves the writeability of the cell while writing '0'. However, the NBL technique is appropriate for the dual bitline cells (e.g. standard 6T/8T) as they always have one low-going store node connected to the bitline while it cannot be applied to the 5T-SRAM cell during write '1' operation.

The BWL technique increases the word line voltage (V_{WL}) connected to the gate of AC transistor (Fig. 2) during write operation. This increases the gate source voltage of AC ($V_{GS\text{-}AC}$) and improves its driveability. However, when writing '1' in asymmetric 5T-SRAM cell, $V_{GS\text{-}AC}$ is determined by the word-line and store node voltages ($V_{GS\text{-}AC}=V_{WL}-V_Q$). Hence, during write '1' operation, $V_{GS\text{-}AC}$ will be decreased by increasing V_Q which leads to significant decrease in access transistor driveability. As a result, the BWL technique is not an effective method to deal with the write '1' weakness of asymmetric 5T-SRAM cells. Hence, there is a need for a write assist technique to improve the writeability of asymmetric SRAM cells which suffer from inability to write '1'.

Cell V_{DD} collapse and cell GND boost techniques can be used in asymmetric single-ended cells in order to improve write '1' and write '0' margins. However, these are much less effective than the NBL write assist technique [25]. On the other hand, these techniques degrade the Hold Static Noise Margin (HSNM) of the half-selected cells and are not suitable for low voltage applications.

To this end, a new asymmetric 6T-SRAM cell is proposed in the following section that improves the write margin and write time. In this cell, a transmission gate is used as the access device.