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High-speed photodiodes in 40 nm standard CMOS technology

M. Atef*, A. Polzer, H. Zimmermann

Vienna University of Technology, Institute of Electrodynamics, Microwave and Circuit Engineering, Gusshausstrasse 25/354, 1040 Vienna, Austria

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ABSTRACT

This work investigates two silicon (Si) photodiodes (PDs) fabricated in 40 nm standard CMOS technology. The basic structure of the proposed Si PD is formed by N+/P-substrate and N-well/P-substrate diodes. The N+/P-substrate PD demonstrates a responsivity of 0.09 A/W and an electrical bandwidth of 3 GHz for 8 V reverse bias at 520 nm. The N-well/P-substrate PD demonstrates a responsivity of 0.24A/W and an electrical bandwidth of 1.2 GHz for 14.8 V reverse bias at 660 nm. For 520 nm, the N-well/P-substrate PD shows a responsivity of 0.18A/W and an electrical bandwidth of 3.0 GHz for 14.8 V reverse bias.

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1. Introduction

The optical receiver is one of the most important building blocks in an optical communication system. The III–V materials have been dominantly exploited for high-speed optical receivers. However, it is an expensive solution compared to silicon technology. Deep sub-micron CMOS technologies have been rapidly advanced, enabling the implementation of integrated optical receivers for data rates of several Gigabits per second. In particular, low-cost silicon CMOS optoelectronic integrated circuits (OEICs) became very attractive because they can be extensively applied to short-distance optical communications, such as local area network, chip-to-chip and board-to-board interconnect. Fully integrated optical receivers with integrated silicon photodiodes provide advantages over hybrid implementations, including low-cost, reduced parasitic capacitance, and no bond-wire inductance.

Unfortunately, the optical absorption coefficient of silicon at 850 nm is quite low. Calculations using the standard photo-generation equations [1] show that the penetration depth of light in silicon is 16.5 μm at 850 nm. This is much deeper than that of the depth of the depletion regions (~2 μm). As a result, a large portion of carriers is generated in the Si substrate and diffuses in all directions. The slow diffusion carriers will reach the depletion region and lead to the slow response of the PN-PD. On the other hand, from the perspective of high-speed light detection, the solution for decreasing the impact from these slow diffusion carriers is the crucial issue and should be circumvented in high-speed monolithically integrated CMOS optical receiver design.

Unfortunately, technology scaling to deep-submicron has a negative impact on the photodiode performance. As the technology shrinks, more metal layers are provided to be able to connect all transistors in a compact way. Thick dielectric stacks are needed to isolate the metal layers from each other and to take care of planarization. So, the transmission coefficient drops quite drastically for technologies with shrinking minimal line widths.

The increased doping levels and lower nominal supply voltages also have a negative impact on the photodiode performance. The width of the space-charge region decreases, as a result the drift current decreases, increasing the diffusion current, increasing the recombination and increasing the parasitic photodiode capacitance for a certain photodiode area. Consequently, the optical as well as the electrical performance becomes worse [2,3].

Test chip was developed to characterize the performance of photodetectors in a 65 nm CMOS technology. The measurements of the N+/P-well/deep N-well photo-transistor with 60 μm × 60 μm in size shows a 3 dB bandwidth of 150 kHz, 9 dB/decade roll-off and responsivity of 0.34A/W. The N+/P-substrate PD shows a 3 dB bandwidth of 2.5 MHz, a roll-off of 5 dB/decade and responsivity of 0.03A/W at 850 nm [4]. The very low bandwidth reported in [4] is a result from the slow carriers' diffusion.

Several techniques are used to reduce the PD slow diffusion currents. One approach is to isolate the photodiode junction from the substrate where the slowest diffusing carriers come. The improvement of photodiode speed comes at the expense of a lower responsivity [5]. Another method to suppress photocurrent slow diffusion components is the spatially modulated light (SML) photodetector. SML photodetector has differential photodiodes consisting of shaded diodes and illuminated diodes. By subtraction of the signals from the illuminated and shaded diodes the cancellation of the partial diffusion photocurrent in the substrate can be

* Corresponding author. Tel.: +43 1 58801 354 600.
E-mail address: mabdelaal@emce.tuwien.ac.at (M. Atef).

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realized [6,7]. The drawback of this SML photodetector is its low responsivity. Not only one-half of the incidents light are reflected away from the covered part of the photodetector but also much of the generated photocurrent is now cancelled by subtraction, resulting in a very low responsivity [8].

The interdigitated network of PW or P+ fingers is another technique can be used to enhance the speed of the photodiode. An interdigitated network of PW or P+ fingers was employed instead of a continuous PW or P+ [1]. This will maximize the depletion regions available for carrier collection, particularly near the surface of the device. A PD using a deep N-well (DNW) with P-well fingers inside and having an active area of 50 μm × 50 μm fabricated in a standard 0.18 μm CMOS process achieved 8.7 GHz −3 dB bandwidth with 0.018A/W responsivity at 850 nm at 11.4 V bias [9].

Avalanche photodiode (APD) can be used to have a high responsivity. An APD based on N+/PW junction was fabricated with 65 nm standard CMOS technology [10]. The design includes shallow trench isolation (STI) between P+ and N+ regions to prevent premature edge breakdown. An optical window with an area of 30 μm × 30 μm is formed by blocking the salicide process. The APD achieved a responsivity of 2.94A/W and 3 dB bandwidth of 3.2 GHz at 850 nm with 10.6 V reverse bias. The high bandwidth and responsivity was achieved in [10] on the expense of higher leakage current and shot noise which will worsens the sensitivity of the optical receiver [11]. The capacitance of the N+/PW PD is larger than the simple N+/Psub PD because of the higher PW doping compared to P-sub doping. A 2.5 pF capacitance was reported in [12] for 80 μm × 80 μm N+/PW PD at 8 V compared to a capacitance of 0.21 pF for 70 μm × 70 μm N+/P-substrate PD (see Section 3.2). The higher N+/PW PD capacitance leads to a smaller bandwidth (RC-limited) at larger PD area required for POF application.

The plastic optical fiber (POF) is a good candidate for short-reach communications and it has 650 nm and 520 nm transmission windows. At these shorter wavelengths the 1/*e* penetration depth of light in silicon is 3.2 μm at 650 nm and 0.75 μm at 520 nm and the absorption coefficient is larger than 850 nm. This smaller penetration depth will reduce the diffusion and most of the absorbed light will generate electron hole pairs exploiting the drift instead of the diffusion transport mechanism.

An integrated photodiode with a diameter of 1 mm for POF application was introduced in [13]. Due to the huge corresponding area of the junction and the relatively high doping concentrations of the used 180 nm CMOS process; the photodiode capacitance is 64 pF at 1.8 V bias. An equalizer was integrated to reach a data rate of 800 Mb/s. The measured responsivity is 0.21A/W for a wavelength of 660 nm.

A 250 μm non-SML NW/P-sub PD implemented in a standard TSMC 65 nm CMOS process was presented in [14] to suit for large core diameter POF. The octagonal PD consists of 56 identical 60 × 15 μm diode strips that are spaced 2 μm apart to satisfy density requirements and allow low-resistance interconnects. The PD shows a simulated responsivity of 0.36A/W, and a 3 dB bandwidth of 60 MHz at 670 nm wavelength. The PD reveals a 10 dB loss at 3 GHz. The PD exhibits a 14 pF capacitance under a 0.3 V reverse-bias voltage.

In this paper two different PDs fabricated in a 40 nm CMOS standard process without any process modifications or design rule waivers will be introduced. The DC and AC characteristics of N+/P-substrate and NW/P-substrate PDs will be shown and discussed for 850 nm, 660 nm and 520 nm wavelengths. The presented PDs have a high performance at wavelengths that are useful for POF application. To the authors knowledge this work presents the first PDs fabricated in 40 nm standard CMOS technology.

2. Photodiode design

Fig. 1 shows the structure of the proposed PDs fabricated in standard 40 nm CMOS process from Taiwan Semiconductor Manufacturing Company (TSMC). In Fig. 1(a) the N+ source/drain implant with the P-substrate are used to implement the PN photodiode. In Fig. 1(b) the N-well with the P-substrate implement another PN photodiode structure. Due to the shallow trench isolation (STI), the breakdown voltages of the N+/P-substrate photodiode is 18.5 V and the breakdown voltage of the NW/P-substrate photodiode is 16.3 V. The STI prevents premature edge breakdown for N+/P-substrate PD but cannot for NW/P-substrate PD because the NW is deeper than the STI. Therefore, the maximum bias voltages of 18 V and 14.8 V were chosen for the N+/P-substrate and the NW/P-substrate photodiode, respectively. The leakage currents for these diodes with an area of 70 μm × 70 μm were 50 nA at these bias voltages.

Each one of the two PDs is designed with different dimensions 30 μm × 30 μm, 50 μm × 50 μm and 70 μm × 70 μm. Due to the

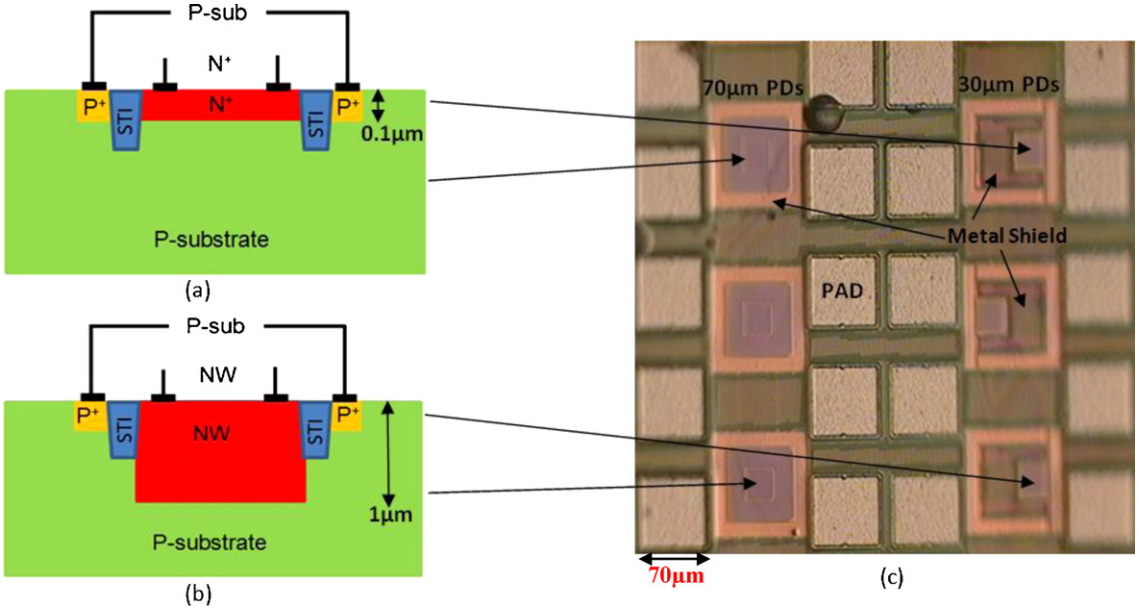

Fig. 1. Photodiode structures (a) N+/P-substrate, (b) NW/P-substrate, (c) die photo for the different photodiode structures with different dimensions.

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