Microelectronic Engineering 88 (2011) 578–582

Contents lists available at ScienceDirect

Microelectronic Engineering

journal homepage: www.elsevier.com/locate/mee

New carbon-based thermal stability improvement technique for NiPtSi used in CMOS technology

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ARTICLE INFO

Article history:
Available online 22 July 2010

Keywords:
NiPt-silicide
Thermal stability
Carbon
CMOS

ABSTRACT

A new carbon-based thermal stability improvement technique is proposed for nickel silicide. Carbon implantation is well known to improve the thermal stability of Ni-based silicides, but its process window is small. An experiment has been performed to identify and introduce new process steps which improve the thermal stability and which can be integrated into a CMOS technology platform without a significant cost increase. No yield issues have been observed up to 700 °C 30 min post-silicidation thermal budget even for the narrowest silicided silicon lines. NiPtSi encroachment, which is one of the main yield killers for Sub-65 nm technologies, has not been seen. The device scalability is not affected and a similar performance has been achieved with an additional post-silicidation thermal budget. Through in-depth understanding of this approach, new integration schemes like for instance a gate-last process flow can be envisioned.

1. Introduction

Since the introduction of the 65 nm CMOS technology node, Nickel (Ni) has replaced Cobalt as the main silicide metal due to its better scalability and resistivity [1,2]. Unfortunately, nickel silicide (NiSi) has a poor thermal stability [3] and improvement is necessary to cope with the substantial post-silicidation thermal budget required by some applications. Platinum incorporation can help (NiPtSi) [3,4], but still remains insufficient for some applications. Some papers [4,5] already proposed different techniques based on impurity implantation to improve the thermal stability. Carbon is one of these elements known to thermally stabilize the NiSi [6,7]. This approach is however not without consequence for the CMOS devices if we consider the fact that a high carbon dose is typically required to enable a large thermal budget after silicidation. Figs. 1 and 2 illustrate device results in case a carbon implantation was used to stabilize the NiPtSi at a low carbon dose the improvement is too small and as the dose is increased, a significant short channel effect (SCE) increase and performance degradation can be observed. The goal of the present study is to enlarge the NiPtSi carbon-based thermal stability improvement process window and to avoid any negative impact on the CMOS device operation.

2. Blanket experiment

First, a blanket experiment has been run to identify the main parameters which could help to obtain better NiPtSi thermal stabilities in comparison to the case of carbon implantation only. To avoid channeling and to keep the C near the silicon surface, pre-amorphization implantation (PAI) was introduced. Afterwards a low thermal budget silicon re-crystallization is needed to have a better silicidation process and at the same time avoid excessive dopant diffusion. This was achieved with millisecond laser annealing (LA). To investigate the role of the PAI, a condition without PAI was introduced. Fig. 3 summarizes the different experimental sequences. For the case with PAI + LA, a higher carbon dose was evaluated as well. After the different sequences, a set of high temperature anneals was given followed by sheet resistance measurement (Rs) and top-SEM to characterize the NiPtSi thermal stability. For all work reported in this paper, the Pt concentration is kept fixed at 5%.

Fig. 4 shows sheet resistance measurements done on P + implanted silicon after silicidation followed by different anneals (similar results were obtained on N + silicon, but are not shown here). Fig. 5 presents a top-SEM picture taken after the anneal at 700 °C. The carbon only route is clearly not sufficient to have a good thermal stability: a significant increase of Rs is observed and a NiPtSi agglomeration is visible after a 700 °C post anneal. Adding the laser anneal (C + LA) or the PAI and LA (PAI + C + LA) clearly improves the sheet resistance but still shows some silicide agglomeration. It is only for the PAI + C + LA with the higher carbon dose that both Rs and top-SEM are okay.

3. Narrow line results

To investigate the impact of the new process sequences on the narrow silicon lines, a similar experiment has been run on pat-

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doi:10.1016/j.mee.2010.07.008

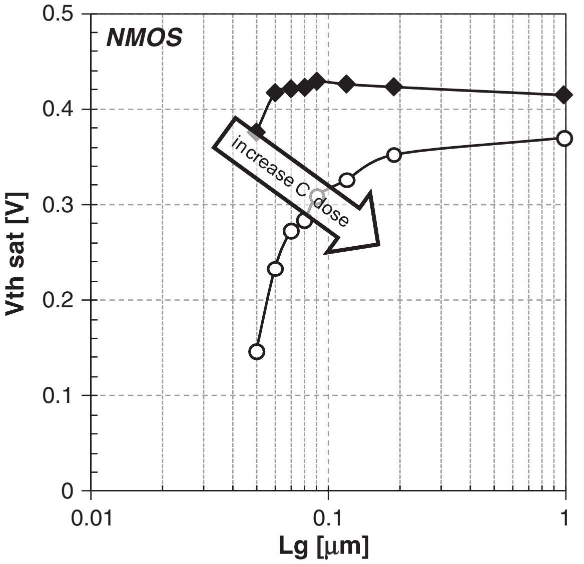

Fig. 1. NMOS Vth versus gate length for different carbon dose used as thermal stability technique.

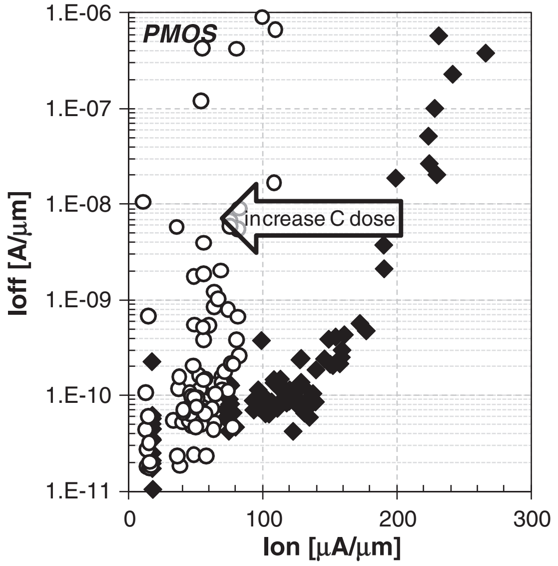

Fig. 2. PMOS Ion versus Ioff for different carbon dose used as thermal stability technique.

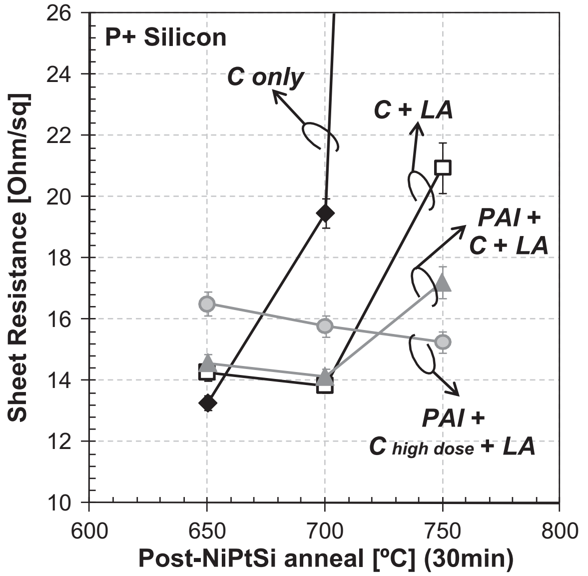

Fig. 4. NiPtSi sheet resistance measurement versus post-silicidation anneal temperature with different thermals stability condition.

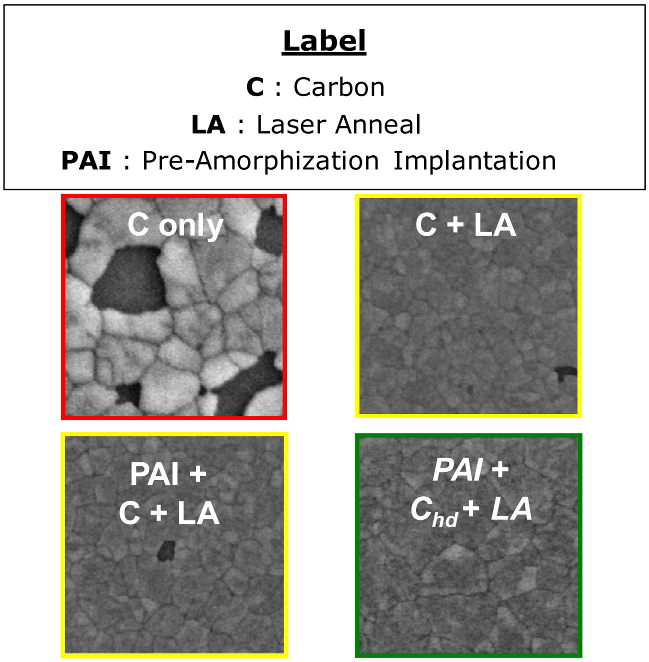

Fig. 5. Top-SEM picture after an 700 °C post-silicide anneal during 30 min with different condition.

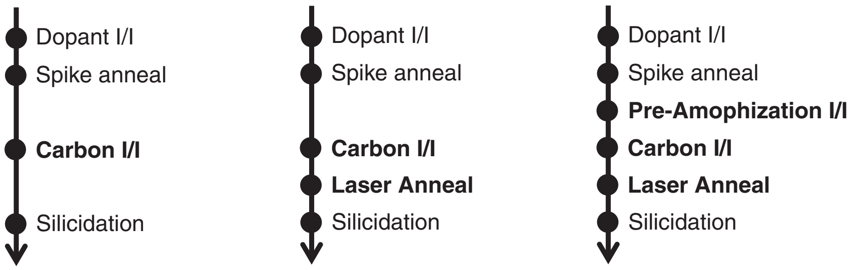

Fig. 3. Blanket experiment summary.