

# Prospect of the future of switched-current circuits with regard to future CMOS technologies

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## Abstract

Low supply voltages in modern CMOS technologies are expected to reduce the maximum resolution of analog to digital converters in voltage mode operation. This paper outlines the functionality and possibilities of switched current (SI) circuit techniques in medium accuracy  $\Delta\Sigma$  modulators. Starting with the presentation of different kinds of switched current cells, this paper gives an overview about the simulated performance followed by a comparison of switched current and switched capacitor circuits. A prospect of the future of switched current circuits with regard to future CMOS technologies is given.

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## 1. Introduction

The increasing complexity of digital circuits forces the use of new technologies. Switching to more advanced technologies offers the possibility to reduce the size and the power consumption and to increase the speed of a digital circuit. A lot of signal processing has been moved from the analog to the digital domain nevertheless basic blocks like analog to digital converters are still needed in modern SoCs. The designer has to build up high precision analog circuits using technologies optimized for digital design.

The increasing transistor speed and the low absolute accuracy of device parameters in modern CMOS technologies leads to the use of delta-sigma analog to digital converters in a wide range of applications. A huge number of switched capacitor (SC)  $\Delta\Sigma$  converters has been developed during the last years. These converters fit very well in the field of medium and high resolution applications. The need of linear floating capacitors not for free available in older digital CMOS technologies supported the

development of MOS-only and switched current (SI)  $\Delta\Sigma$  modulators. Although much effort in SI development, the limited accuracy of SI memory cells remains the main obstacle of this circuit technology. The number of publications in this area of research decreased some years ago because of this limitation.

Some comparison on switched current and SC circuits in different technologies were made in [1–3,23]. These papers concentrate on basic sample-and-hold circuits and compare the SNR and a figure of merit in different circuit and CMOS technologies. The reported results are based on extrapolation of future technology parameters. Different integrator structures are used in SC and SI  $\Delta\Sigma$  converters. The performance of medium accuracy switched current  $\Delta\Sigma$  modulators cannot be extrapolated from 2 transistor sample-and-hold circuits. A comparison between SI and SC modulators has to focus on the speed and accuracy of the integrator building block.

The reduction of supply voltage in modern CMOS technologies drives the design of SC circuits into a number of problems like reduction of signal swing and reduced transconductance of switches. This change of technology parameters may be able to open a niche for switched current high speed medium resolution  $\Delta\Sigma$  converters. In future it may be possible that this circuit technique is able

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to outperform SC or continuous time solutions in one or two performance parameters.

This paper faces the prospects and problems of SI circuit technique for medium resolution  $\Delta\Sigma$  ADCs. In Section 2 different SI memory cells and integrators as main building blocks of an  $\Delta\Sigma$  ADC are presented. An overview about state of the art designs and performance is given in Section 3 followed by a comparison of switched current and SC  $\Delta\Sigma$  ADCs in Section 4. The future of SI ADCs in modern technologies is presented in Section 5.

## 2. SI circuits

### 2.1. Basic memory cell

A basic class A switched current memory cell is shown in Fig. 1. The P-MOS transistor M2 is working as a current source generating the bias current  $I_{bias}$ . During the first clock phase M1 is diode connected. The drain current of M1 is the sum of the input current and  $I_{bias}$ . Because of disconnecting the gate of M1 in the second clock phase, the gate source voltage remains constant and so the drain current. The output current  $I_{out}$  of the cell equals  $-I_{in}$ .

This simple configuration has only low accuracy because of channel length modulation, charge injection, clock feed-

through and other parasitic effects. Different circuits have been developed to overcome these problems.

### 2.2. Advanced memory cells

All presented cells focus on the main error source of the basic memory cell—channel length modulation. There are two solutions which are commonly used. The first one is cascoding the memory transistor like shown in Figs. 2 and 3. The second possibility is to reduce the voltage swing at the drain of the memory transistor by using grounded gate configurations. Possible circuit realizations are shown in Figs. 4 and 5.

The introduced feedback loop improves the accuracy but also reduces the maximum clock speed of these cells. Simulations of the presented cell types showed that the cascoded memory cell is the best choice for high speed operation. The reported accuracy of SI AD converters using improved memory cells is still limited to around

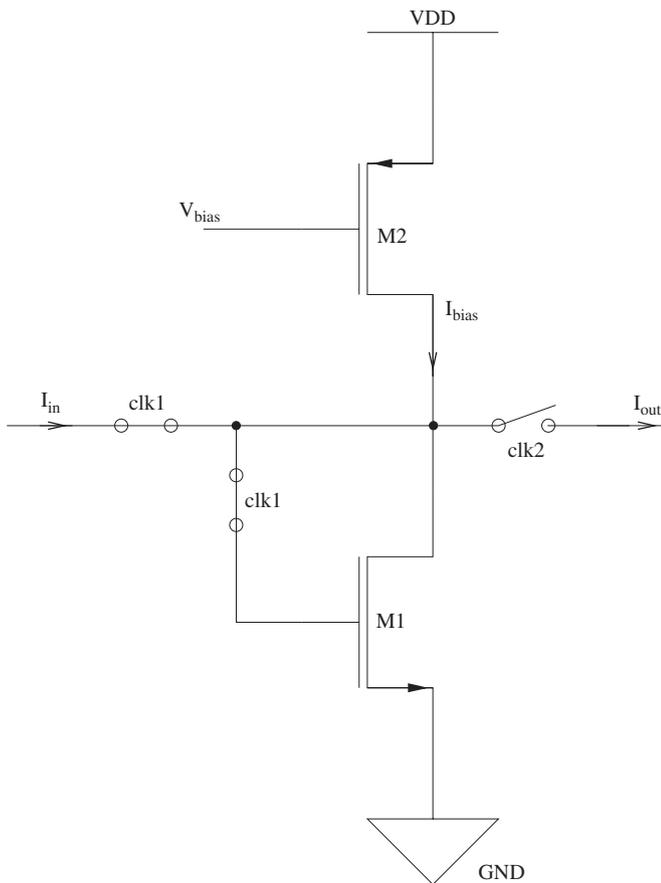


Fig. 1. Basic switched current memory cell.

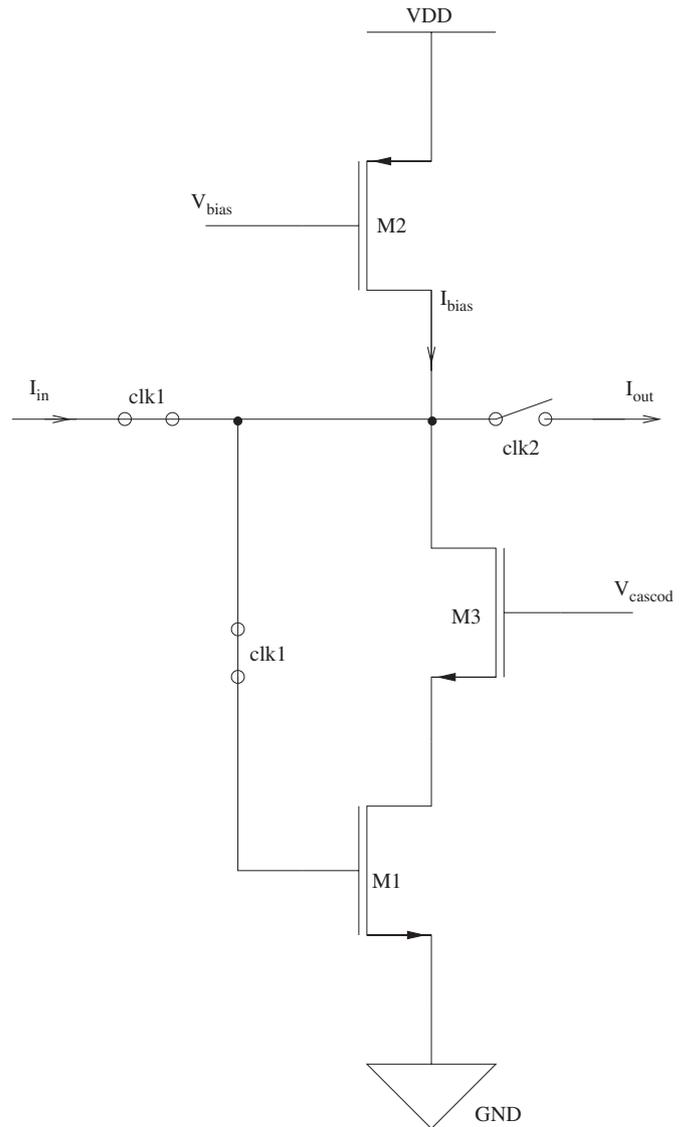


Fig. 2. Cascoded switched current memory cell.

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