



## Review of fuse and antifuse solutions for advanced standard CMOS technologies ☆

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### ABSTRACT

Specific applications require large amounts of high-performance, dense and low-cost non-volatile memories with CMOS standard process compatibility. There exists numerous structures for one-time-programming (OTP) bitcells, exploiting various physical phenomena as programming modes. Not all of these physical phenomena will behave in a satisfactory manner with the CMOS technology shrink. Moreover, it is not easy to evaluate the effect of geometry and technology on the trade-off between density and reliability of the OTP bitcells.

This paper aims to review literature about OTP memories and show that metal fuse, polyfuse and antifuse are the best candidates so far. Other memories require either additional masks with regards to core process, additional technological steps or unaffordable programming conditions. Significant results will be listed in comparison tables.

This paper also wishes to give a summary of the physical phenomena involved in bitcell architectures. Opinions are given about the suitability of OTP architectures for specific applications, the most suitable bitcell architectures have been layouted in 65 and 45 nm for density comparison purpose. Particularly, promising structures are manufactured and characterized as they present fair trade offs for standard CMOS process. Discussion and conclusion are intended to give a comprehensive review about the parameters impacting the performances, the density and the cost of the OTP bitcell. Comparison tables are edited with the most pertinent parameters and available results.

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### 1. Introduction

System-on-chips (SoCs) gather many functional blocks, all CMOS compatible. The dispersion in manufacturing implies to repair, tune or calibrate some parts. Other parts need to be personalized or programmed. Fuses are then used in many applications due to their low-cost manufacturing and full compatibility with CMOS SoC. Main applications are:

- Code storage for security or cryptography.
- Embedded-RAM repair [1,2] (the increase in manufacturing variability with advanced technologies presses for the development of fuses).

- Analogue block trimming: laser or zener zapping are no more adapted to wafer-level test and advanced technologies so fuses represent a promising alternative [3].
- Setting digital functions.

At the dawn of CMOS 32 nm and beyond, it is necessary to develop and mature new solutions of fuses and more generally OTPs. The challenges for new OTP memories are high density, high reliability, high memory capacity, low programming voltage, low programming current, speed at least as good as standard flash memories and compatibility with standard CMOS process for systems-on-chip development, i.e. no additional mask for low cost manufacturing.

Various types of OTP, usually integrated at front end level, have been reported. Floating gate memories are specific memories which can be used as OTP. Thanks to their floating gate which can store charges, they can be written and erased many times. A single polysilicon floating gate is presented in [4] that is standard CMOS process compatible. A coupling capacitor is associated to a tunnelling capacitor for operations of the bitcell. Programming is performed by capacitive coupling and erasing is based on Fowler Nordheim mechanism. A minimal area of these capacitors

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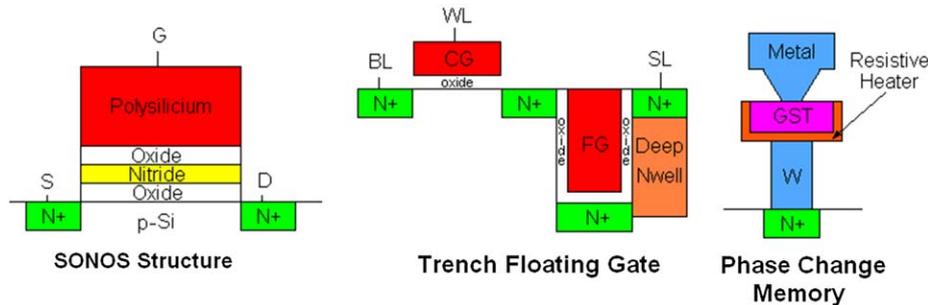
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**Table 1**  
Floating gate and emerging memories: key-points.

Bitcell	SONOS [20]	PCM [9]	SimplEE [22]	Single floating gate [6]	Gateless [8]
Techno	0.18 $\mu\text{m}$	0.18 $\mu\text{m}$	0.35 $\mu\text{m}$	0.25 $\mu\text{m}$	45 nm
Area ( $\mu\text{m}^2$ )	0.40	0.32	4	265 <sup>a</sup>	0.449
Prog. voltage (V)	–8	– <sup>b</sup>	13	6.5	–5
Prog. time ( $\mu\text{s}$ )	10	–	–	100	30
Cut	4 Mb	8 Mb	64 kb	32 b	–
Data retention	–	–	150 °C 30 years	85 °C 10 years	48.9 °C 10 years
Add. mask	+6	Yes	Yes	0	0

<sup>a</sup> Area by bit with peripheral circuits. Ref. [6] shows an area  $< 0.0085 \mu\text{m}^2$  for 32 bits.

<sup>b</sup> Empty cases: data not given in publications.



**Fig. 1.** Technological schematics of pertinent bitcells.

has to be kept whatever the technology shrink. There is also an immediate impact on density, and probably reliability due to oxide thickness reduction. In [5], another single polysilicon bitcell is presented with the aim to improve programming characteristics by hot electrons. They use a NMOS with a gate not silicide-coated on drain side and P+ implanted on source side. This introduces a difference of work functions which improve channel's hot electron programming. A PMOS single floating gate is presented in [6] in 0.25  $\mu\text{m}$  CMOS standard process. Channel hot-electrons are injected and stored in the PMOS floating gate, changing its threshold voltage. This paper demonstrates good electrical performances and reliability. Nevertheless, the drawbacks are density (265  $\mu\text{m}^2$  by bit) and data retention not assured in advanced technologies.<sup>2</sup>

Generally, the oxide thickness issue remains the main limitation of these structures with the technology shrink. Data retention on floating gate becomes a reliability issue for oxide thicknesses  $< 50 \text{ \AA}$  which would be unavoidable in advanced technologies [7].

A solution to prevent from this problem is not to use floating gate. Recently, [8] has presented a gateless OTP cell. They replace PMOS floating gate by floating RPO (resist-protection oxide). Nevertheless, reliability and more particularly data retention is not guaranteed for temperature higher than 50 °C and no memory cut has been demonstrated.

New emerging OTPs appear like phase change memory [9–13] (PCM), semiconductor–oxide–nitride–oxide–semiconductor (SONOS) memories [14,15] and resistive random access memory (R-RAM or ReRAM) [16]. PCM mechanism is based on the state of a chalcogenide material. When its state is amorphous, its electrical resistance is high and when it is in crystalline state, its electrical resistance is low. Self-heating due to electrical conduction is used to change the state of the chalcogenide material. R-RAM is based on binary metal oxides such as  $\text{TiO}_2$ , NiO. The mechanism uses resistance switching. At low voltage, a conductive path appears in the metal oxide. At high voltage the conductive path is broken and

the resistance increases. This memory has all the advantages (quicker, low consumption) to replace flash memory. But binary metal oxides need additional processes steps and masks, hence are not adapted for low cost OTP memories. SONOS memories present a nitride layer inside the gate oxide and charges are stored inside this nitride layer instead of polysilicon layer. These memories are said to replace next generation double-poly Flash memories but the nano-crystal oxide ( $\text{SiO}_x$ ) memory is also a serious alternative [17,18]. Whatever, these memories can be written and erased many times, but their process is mainly non-standard CMOS process compatible (6 additional masks) [19] and require quite large areas, and are thus not adapted for low cost OTP.

Table 1 gives some key parameters for comparison of several flash and emerging memories: SONOS [20,15], PCM [9,12], a buried trench Floating-Gate [21], a simple Floating-Gate memory, SimplEE [22], a single PMOS floating gate [6] and a gateless bitcell [8]. Literature gives only few details but sufficiently to observe that most structures are quite similar from performance point of view except those described in [22] (extra large area).

Other floating-gate structures have been demonstrated (stacked gate or split gate [23]) but they are clearly more complex from manufacturing point of view. Fig. 1 pictures the technological structures of the latter bitcells. Considering the performance, these architectures are probably scalable to CMOS 32 nm or beyond. However, additional masks with respect to core process will remain necessary and make them non-suitable for the development required by SoCs.

The most promising solutions are then based on the alteration of the physical or chemical property of a material:

- If a layer is an electrical conductor and programming blows this property: it is called a fuse.
- If a layer is not a conductor and programming initiates electrical conduction: it is called an antifuse.

The solutions should be compatible with CMOS technologies if the selected material belongs to the standard manufacturing process. Moreover the solutions are inherently scalable.

<sup>2</sup> With peripheral circuits. Ref. [6] shows an area  $< 0.0085 \mu\text{m}^2$  for 32 bits.

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