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High linearity, low power RF mixer design in 65 nm CMOS technology

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ABSTRACT

A design of RF down-conversion Gilbert-Cell, with 65 nm CMOS technology, at a supply voltage of 1.8 V, with a new degenerating structure to improve linearity. This architecture opens the way to more integrated CMOS RF circuits and to achieve a good characteristics in terms of evaluating parameters of RF mixers with a very low power consumption (2.17 mW). At 1.9 GHz RF frequency; obtained results show a third order input intercept point (IIP3) equal to 11.6 dBm, Noise Figure (NF) is 4.12 dB, when conversion gain is 8.75 dB.

1. Introduction

Since several years, research for possibilities of CMOS technologies for RF applications is growing enormously. The trend toward deep sub-micron technologies allows the operation frequency of CMOS circuits above 1 GHz, which opens the way to miniaturize integrated RF circuits while reducing energy consumption.

The Mixer block has a critical impact on the performances of all system functions in any RF channel. It is a non-linear device used to translate one frequency to another. On receiver chain (Fig. 1), on which we worked, the principle of any type of RF mixer is that the Local Oscillator (LO) drives by (switching/modulating) the incoming Radio Frequency (RF) to an Intermediate low Frequency (IF) [1].

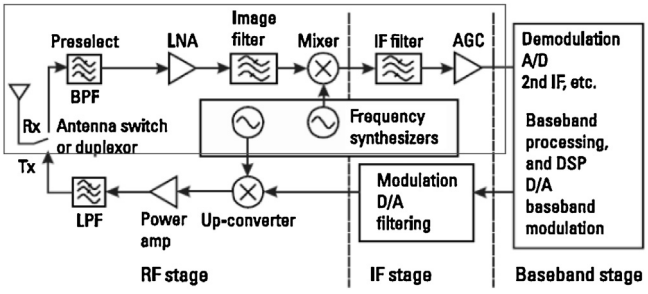

Fig. 1. Typical transceiver block diagram [1].

This work reports a design of Gilbert cell mixer with 65 CMOS technology, starting by the architecture of proposed circuit, then a theoretical study to improve linearity, and simulation result of evaluating parameters on ADS tool, also a potential comparison with recents proposed circuits.

2. Architecture of proposed mixer

2.1. Mixer operation

Gilbert Cell is a double balanced mixer, much complex, but have more performances compared to single balanced mixer: all ports of the mixer are inherently isolated from each other, increased linearity, and improved suppression of spurious products than less susceptible to supply voltage noise due to differential topography [2].

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As shown in Fig. 2, RF signal is applied to the transistors (M2 and M3) which perform a voltage to current conversion. MOSFETs M4–M7 form a multiplication function of the linear RF signal current from (M2 and M3) with LO signal applied across M4–M7.

(M2 and M3) provide ±RF current and (M4 and M6) switch between them to provide the inverted RF signal to the left hand load. (M5 and M7) switch between them for the right hand load. The two load resistors form a current to voltage transformation giving a differential output IF signals [2].

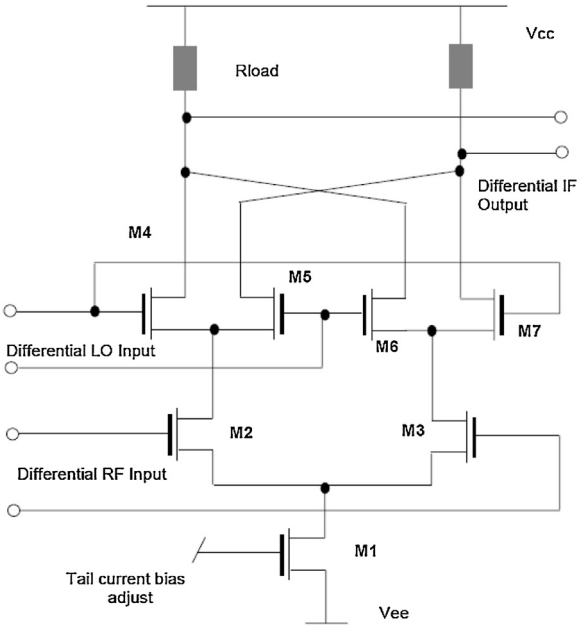

Fig. 2. Gilbert cell architecture.

2.2. Choice of CMOS 65 nm technology

The 65 nm length of MOSFET channels was chosen to maximize gain, to minimize noise and to optimize the footprint of the circuit. The width was chosen maximum with respect to current consumption specifications [3].

Length and width of input RF CMOS block dedicated to analog/RF applications is determined, using a technique based on the minimum noise to obtain optimal size of the width, that is expressed by the following equation [4]:

$$W = W_{opt} = \frac{1}{3\omega L R_s C_{ox}} \tag{1}$$

where W and L are respectively the width and the length of MOS channel. C_{ox} is the surface capacitor of the gate-channel and R_s is the resistor of matching (generally equal to 50 Ω). Then, an adjustment is made after the simulation to achieve the desired performances.

2.3. Improving linearity circuit

Gilbert Cell Mixer Linearity depends on the three main sources: RF stage, switching and load circuits. On general, linearity is represented by intermodulation (IM3) performances: this parameter is measured by applying the third order products from the mixing of RF and LO tones with the LO tones at the frequencies given by: (2RF ± LO) ± LO and (2LO ± RF) ± LO. Generally the most interesting third other product are: (2RF-LO)-LO and (2LO-RF)-LO as they fall in, or close to the IF band [2].

2.3.1. Third harmonic relative to the fundamental

Input attacks a differential pair, as shown in Fig. 3:

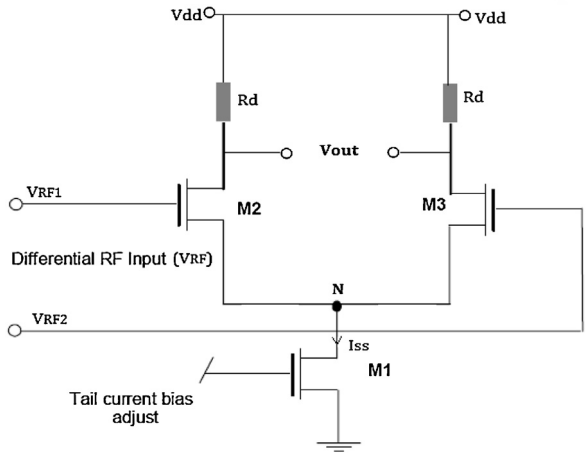

Fig. 3. Double balanced mixer circuit.

V_{RF} and V_{out} being a differential tensions: $V_{RF} = V_{RF1} - V_{RF2}$ and $V_{out} = V_{out1} - V_{out2}$

I_{D3}, I_{D2} are respectively the drain currents of transistors M_3 and M_2, with:

$$V_{out} = R_D(I_{D2} - I_{D3}) \tag{2}$$

The potential at N point is equal both to $V_{RF1} - V_{GS1}$ and $V_{RF2} - V_{GS2}$ thus:

$$V_{RF1} - V_{RF2} = V_{GS1} - V_{GS2} \tag{3}$$

Given that [4]:

$$V_{GS} = \sqrt{\frac{2I_D}{\mu_n C_{ox}(w/L)}} + V_{TH} \tag{4}$$

Then:

$$V_{RF1} - V_{RF2} = \sqrt{\frac{2I_{D2}}{\mu_n C_{ox}(w/L)}} - \sqrt{\frac{2I_{D3}}{\mu_n C_{ox}(w/L)}} \tag{5}$$

Our objective is to determine the amplitude ratio of third harmonic of the output signal (V_{out}) relative to the fundamental. Based on Eq. (2) we just need to calculate ($I_{D3} - I_{D2}$).

By squaring expression (5), we obtain:

$$(V_{RF1} - V_{RF2})^2 = \frac{2}{\mu_n C_{ox}(w/L)}(I_{ss} - 2\sqrt{I_{D3}I_{D2}}) \quad \text{with } I_{ss} = I_{D3} + I_{D2} \tag{6}$$

Given that:

$$4I_{D3}I_{D2} = (I_{D3} + I_{D2})^2 - (I_{D3} - I_{D2})^2 = I_{ss}^2 - (I_{D3} - I_{D2})^2$$

By squaring expression (6) and after a serie of simplifications, we obtain

$$I_{D2} - I_{D3} = \frac{1}{2}\mu_n C_{ox}(w/L)V_{RF}\sqrt{\frac{4I_{ss}}{\mu_n C_{ox}(w/L)} - V_{RF}^2} \tag{7}$$

I_{ss} being equal to the double of drain current of transistors, Eqs. (7) and (3) lead to:

$$I_{D2} - I_{D3} = \frac{1}{2}\mu_n C_{ox}(w/L)V_{RF}\sqrt{4(V_{GS} - V_{TH})^2 - V_{RF}^2}$$

$$= \mu_n C_{ox}(w/L)V_{RF}(V_{GS} - V_{TH})\sqrt{1 - \frac{V_{RF}^2}{4(V_{GS} - V_{TH})^2}} \tag{8}$$