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Electrical characterization of thulium silicate interfacial layers for integration in high-k/metal gate CMOS technology

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ABSTRACT

This work presents a characterization of the electrical properties of thulium silicate thin films, within the scope of a possible application as IL (interfacial layer) in scaled high-k/metal gate CMOS technology. Silicate formation is investigated over a wide temperature range (500–900 °C) through integration in MOS capacitor structures and analysis of the resulting electrical properties. The results are compared to those obtained from equivalent devices integrating lanthanum silicate interfacial layers. The thulium silicate IL is formed through a gate-last CMOS-compatible process flow, providing IL EOT of 0.1–0.3 nm at low formation temperature and interface state density at flatband condition below 2×10^{11} cm^{-2} eV^{-1}. The effects of a possible integration in a gate-first process flow with a maximum thermal budget of 1000 °C are also evaluated, achieving an IL EOT of 0.2–0.5 nm, an interface state density at flatband condition $\sim 1 \times 10^{11}$ cm^{-2} eV^{-1} and a reduction in gate leakage current density of one order of magnitude compared to the same stack without IL.

1. Introduction

High-k/metal gate technology has been introduced in the CMOS device scaling roadmap in order to overcome the inherent limitation in the scalability of conventional SiO_2 and SiON gate dielectrics, where aggressive scaling of the physical thickness results in an exponential increase in gate leakage current density [1]. Alternative gate dielectrics have been researched with a dielectric constant which is high enough for the leakage current to be kept at an acceptable level while still achieving a high capacitance density, or equivalently a low EOT (equivalent oxide thickness). The most widespread high-k dielectrics in current CMOS technology are Hf-based oxides, which provide a relative dielectric constant in the range 17–30 [2]. Alternative materials for integration in future technology nodes are also actively researched, with a strong focus on lanthanide oxides [1]. Integration of high-k dielectrics in CMOS technology requires the introduction of a multi-layer gate stack, where each layer mainly addresses one objective of the overall gate stack design [3]. The main high-k layer provides high dielectric constant and high physical thickness, with the purpose of achieving low EOT and low leakage current density. An interfacial layer (IL) is usually present between the main high-k oxide and the underlying semiconductor, with the purpose of improving the quality of the interface with the channel. A capping layer is often integrated between the main high-k layer and the metal electrode, with the purpose of modulating the effective workfunction and obtaining symmetric N- and P-MOSFET threshold voltages, which is necessary for CMOS logic circuit operation. State-of-the-art CMOS technology employs Hf-based dielectrics as the main high-k oxide layer, since they provide high dielectric constant and can achieve suitable N- and P-MOSFET threshold voltages through integration of La- and Al- based capping layers and/or through integration of TiAlN and TiN metal electrodes [1]. Hf-based dielectrics are deposited on top of a sub-nm chemical oxide or oxynitride (SiO_x or SiON) interfacial layer, whose thickness is critical for the scalability of the stack [4]. Low and controlled IL thickness can be obtained by different oxidation methods [5,6] and can be further reduced through properly designed scavenging steps. Integration of scavenging elements in the dielectric and metal layers has been demonstrated, showing a reduction in interfacial layer thickness upon annealing [7]. Independently of the specific method employed, a general trend has been observed correlating the decreasing interfacial layer thickness to strong degradations of the inversion layer mobility [7,8]. Even stronger degradations in terms of mobility and reliability have been observed for Hf-based gate stacks which do not employ an interfacial layer [9]. Interfacial layer thickness is thus a crucial tradeoff in the design of current high-k/metal gate stacks [1].

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Integration of a high-k interfacial layer would overcome the tradeoff on IL physical thickness and could extend the scalability of the gate stack, provided that the quality of the interface towards Si is comparable to what can be obtained with chemical oxide and oxynitride interfacial layers and that the high-k IL does not cause additional degradation in inversion layer mobility and device reliability. The material class of silicates is capable of meeting these requirements and a considerable amount of research has been devoted to investigating and optimizing the formation of silicates by reaction of a lanthanide oxide with the underlying silicon [10]. Lanthanum silicate ($La_xSi_yO_z$, "LaSiO" hereafter) formation has been widely studied and the LaSiO/La_2O_3 dielectric stack has been integrated in MOS capacitors and transistors, achieving low EOT with high mobility and low interface state density [11,12]. The main obstacles to the integration of this material system in a CMOS process consist in the hygroscopic nature of La_2O_3 and its fairly strong reactivity with Si. Integration of a hygroscopic La_2O_3 high-k dielectric increases process complexity (since it requires *in situ* deposition of capping layer and/or metal gate and avoiding any exposure to air [11]) and causes concerns in terms of long term reliability. Strong reactivity with Si means that the LaSiO thickness is strongly dependent on the annealing conditions and that a scaled EOT of the IL can only be achieved when the silicate formation is performed in PMA (post metallization anneal) after deposition of a properly designed metal or MIPS (metal inserted poly silicon) stack [12]. This type of process flow for silicate formation renders the integration of LaSiO as IL in a conventional Hf-based gate stack virtually impossible and restricts its applicability to La-based gate stacks.

The advantage of combining a high-k lanthanide silicate IL with existing Hf-based process technology can be achieved by selecting a lanthanide oxide which can form a thin silicate in PDA (post deposition anneal) and does not impose processing constraints in terms of *in situ* process flows and specific design of the gate stack. This work demonstrates a CMOS-compatible process flow for integration of thulium silicate ($Tm_xSi_yO_z$, "TmSiO" hereafter) as interfacial layer in a generic gate stack. Electrical characterization is performed on MOS capacitors integrating a TmSiO IL formed at varying PDA temperature and compared to results obtained from similar devices employing a LaSiO IL. Possible integration of the silicate IL in both a gate-last and a gate-first process flow is investigated, by evaluating the effects of a PMA performed at varying temperature on the properties of the interfacial layer.

2. Silicate formation

The silicate IL process flow has been designed with the purpose of being able to replace the conventional SiO_x or SiON interfacial layers in a generic gate stack. The silicate IL should therefore be formed prior to the deposition of the main high-k layer and the process should facilitate a straightforward integration, without requiring *in situ* processing. The silicate IL process flow has been designed as a three-step process:

(1) *Oxide deposition:* while different techniques can in principle be used, ALD (atomic layer deposition) is the preferred method, since it allows deposition of thin layers with the required uniformity and conformality.
(2) *Silicate formation:* forming the silicate in post deposition anneal facilitates the integration of the IL in a generic gate stack and decouples the silicate formation temperature from the high-k/metal gate thermal budget.
(3) *Removal of unreacted oxide:* the remaining unreacted oxide needs to be removed selectively towards the formed silicate. Compatibility of the etching strategy with standard CMOS materials is also necessary.

Selection of a suitable material for integration as high-k IL should follow different criteria than those for the selection of the main high-k layer. The primary research criteria in exploring the space of possible material candidates for high-k interfacial layers reflect the main role of the IL in a multi-layer gate stack, i.e. providing a good electrical quality of the interface with the underlying silicon and not introducing additional mobility degradation compared to SiO_x and SiON interfacial layers. Materials that do not meet the requirement of high dielectric constant for integration as main high-k dielectric can still be potential candidates for integration as IL, as long as they can achieve an EOT of the IL that is competitive with state-of-the-art SiO_x and SiON interfacial layers.

LaSiO has been shown to fulfill the requirements for integration as IL when the silicate is formed by annealing a La_2O_3 film which has been previously *in situ* capped with a metal or MIPS stack [10–12]. The requirements for *in situ* processing and silicate formation in PMA stem from the fairly strong reactivity of La_2O_3 with Si and its hygroscopic nature. When LaSiO is formed via the process flow proposed in this work, these two properties make it difficult to achieve a low physical thickness of the IL and to prevent degradation of the dielectric constant due to hydroxylation. However, reactivity with Si and hygroscopicity tend to decrease with increasing atomic number among lanthanides [13,14]. Therefore, TmSiO stands as a possible candidate IL, since Tm_2O_3 shows good properties in terms of dielectric constant [15] and conduction and valence band offsets [16] among high-atomic-number lanthanide oxides and TmSiO provides a relatively high dielectric constant (10–12 [15], similar to LaSiO [10]).

3. Experiment

3.1. Fabrication of MOS capacitors

P-type (B doped, 20–40 Ω cm) Si (100) substrates were processed according to the following steps (Fig. 1):

1. *Cleaning:* the substrates were cleaned in H_2SO_4:H_2O_2 (3:1) and HF 5%.
2. *Oxide deposition:* ALD was performed in a Beneq TFS 200 system. One of the two following oxide depositions was performed on each sample:
   (a) *La_2O_3:* La_2O_3 was deposited at 250 °C using La(^{i}PrCp)$_3$ and H_2O as precursors.
   (b) *Tm_2O_3:* Tm_2O_3 was deposited at 250 °C using $TmCp_3$ and H_2O as precursors.

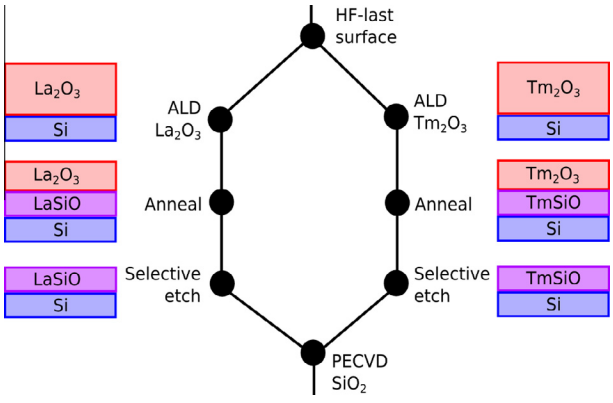

Fig. 1. Process flow of the gate dielectric stack. The interfacial layer is formed by depositing either Tm_2O_3 or La_2O_3 on HF-last Si, followed by silicate formation annealing and removal of unreacted oxide in H_2SO_4. Subsequently, the top oxide layer is deposited, in this case PECVD SiO_2.