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High mobility CMOS technologies using III–V/Ge channels on Si platform

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ABSTRACT

MOSFETs using channel materials with high mobility and low effective mass have been regarded as strongly important for obtaining high current drive and low supply voltage CMOS under sub 10 nm regime. From this viewpoint, attentions have recently been paid to Ge and III–V channels. In this paper, possible solutions for realizing III–V/Ge MOSFETs on the Si platform are presented. The high quality III–V channel formation on Si substrates can be realized through direct wafer bonding. The gate stack formation is constructed on a basis of atomic layer deposition (ALD) Al_2O_3 gate insulators for both InGaAs and Ge MOSFETs. As the source/drain (S/D) formation, Ni-based metal S/D is implemented for both InGaAs and Ge MOSFETs. By combining these technologies, we demonstrate successful integration of InGaAs-OI nMOSFETs and Ge p-MOSFETs on a same wafer and their superior device performance.

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1. Introduction

It has been well recognized that new device engineering is indispensable in overcoming difficulties of advanced CMOS and realizing high performance LSIs under 10 nm regime. Here, the channel materials with high mobility and, more essentially, low effective mass, are preferable under quasi-ballistic transport expected in ultra-short channel regime [1]. From this viewpoint, strong attentions have recently been paid to Ge and III–V semiconductor channels. Because of extremely high electron mobility and low electron effective mass of Ge and III–V semiconductors such as GaAs, InP, InGaAs and InAs and extremely high hole mobility and low hole effective mass of Ge, Ge and III–V materials are suitable for high performance CMOS applications. The ITRS 2011 is predicting that the timeline for introducing Ge and InGaAs channels is set at 2018 [2].

One of the ultimate CMOS structures can be the combination of III–V nMOSFETs and Ge pMOSFETs, as shown in Fig. 1 [1,3,4]. Here, MOSFETs using these materials must be fabricated on Si substrates in order to utilize Si CMOS platform, meaning the necessity of the co-integration of III–V/Ge on Si, which is often called heterogeneous integration. Also, those channels must be ultrathin body structures such as ultrathin films, Fin structures or nano-wire structures, because of the suppression of short channel effects. The gate stacks composed of high k gate insulators and metal gates are regarded as mandatory for scaled CMOS. The formation of source/drain (S/D) regions with low resistance and leakage current is also a critical issue for ultrathin body structure. One promising structure is metal S/D, which inherently provides the low S/D resistance.

Here, one of the most important requirements of III–V/Ge channel MOSFETs on the Si platform is to form these channel materials with high crystal quality on a large size Si wafer, in order to fully utilize the present Si CMOS platform and to realize LSIs. This is because the advanced fabrication facilities and LSI design platform are mandatory for realizing highly-integrated systems. As a result, the co-integration of the III–V and Ge channel materials on a Si substrate, in other words, the heterogeneous integration, is indispensable. Fig. 2 shows a variety of possible applications of III–V/Ge materials on the Si CMOS platform [4]. The CMOS devices using those non-Si material channels are corresponding to the so-called More Moore approach pursuing for higher current drive. There are currently many possibilities in the CMOS configuration. III–V n-MOSFET and Ge p-MOSFET can be combined with strained-Si devices, aggressively developed so far. Also, if high performance Ge n-MOSFET or III–V p-MOSFET are realized, Ge CMOS or III–V CMOS is also viable in terms of the simplicity of the channel structures. Also, one of the ultimate CMOS structure can be a combination of III–V channel n-MOSFET and Ge channel p-MOSFET [3], as proposed in Fig. 1. Which device structures will be adopted is strongly dependent on the progress in the device technologies of each MOSFET and the integration technologies and, finally, on the balance between the performance merit and the fabrication cost.

This heterogeneous integration is, on the other hand, expected to create novel LSIs or SoC utilizing a variety of device families

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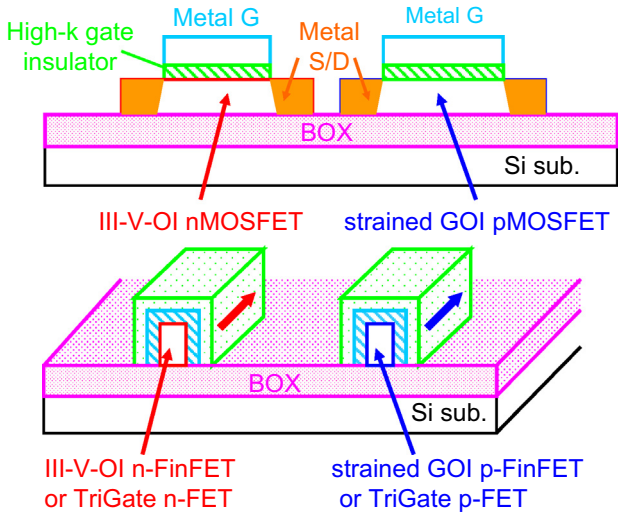

Fig. 1. Ultimate CMOS device structure composed of III–V nMOSFET and Ge pMOSFET.

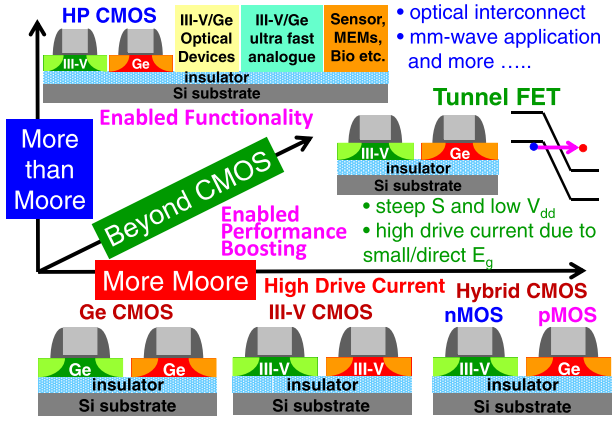

Fig. 2. Possible evolution scenario for III–V/Ge devices on Si platform through heterogeneous integration.

along the More-than-Moore and the Beyond-CMOS approaches, in addition to the More-Moore approach, as seen in Fig. 1. One typical example of the beyond CMOS devices is tunneling FETs aiming at ultra-low power applications. However, one of the drawbacks of the tunneling FETs is the low drive current due to low tunneling probability of electron through the band-gap. Since Ge and InGaAs have the lower band-gap than Si, the much higher on-current is expected in tunneling FET using these channel materials [5,6].

Also, Ge and III–V materials are more suitable for optical devices and ultra high frequency analog devices. In addition to them, a variety of functional devices based on non-Si materials can be integrated with Si digital CMOS, leading to new SoCs along the More-than-Moore approach. Possible near-term applications could be (1) integration with optical interconnects by using Ge or III–V optical devices like detectors and modulators (2) integration with ultra-fast III–V analog devices. As a result, the heterogeneous integration can be expected to yield various and versatile semiconductor chips and markets. Among these applications, the most fundamental device structure is Ge/III–V MOSFETs on Si substrates.

In order to realize this CMOS structure, however, there are still many technological issues to be solved for realizing Ge/III–V MOSFETs on Si substrates. Fig. 3 summarizes critical issues for realizing III–V/Ge MOSFETs on the Si platform, which are listed as follows

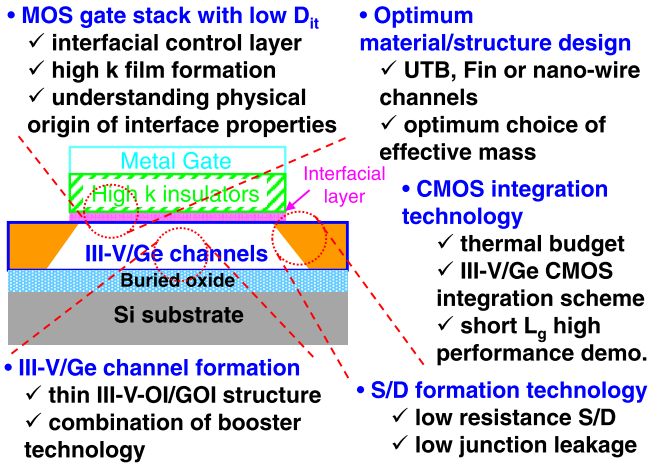

Fig. 3. Critical issues for realizing III–V/Ge MOSFETs on the Si platform.

[3,4]; (1) high quality Ge/III–V film formation on Si substrates (2) gate insulator formation with superior MOS/MIS interface quality (3) low resistivity source/ drain (S/D) formation (4) total CMOS integration. It should be noted here that the ultrathin body Ge/III–V channels such as extremely-thin-body-on-insulator structures, Fin structures and nano-wire structures are mandatory for applying Ge/III–V MOSFETs to scaled CMOS in order to suppress short channel effects (SCEs).

In this paper, we present several possible and viable solutions for the above critical issues. First, we give several technologies for realizing III–V MOSFETs on Si substrates and present the device properties. Next, we touch on the Ge gate stack technologies, which is one of the critical issues of Ge MOSFETs. Finally, we present an example of the integration of Ge and III–V MOSFETs on a same wafer through the combination of the developed fabrication technologies.

2. III–V mosfet technologies

The high quality III–V channel formation on the Si platform is very challenging. While there are many approaches in III–V channel formation on Si such as wafer-level hetero-epitaxy [7–9], selective hetero-expitaxy [10–15] and epitaxial transfer [16,17], we are currently employing the direct wafer bonding (DWB) process of InGaAs/InP wafers with Si substrates for fabricating the InGaAs-on-Insulator (InGaAs-OI) substrates [18–29]. ECR-plasma SiO_2 [18,19,24] and ALD Al_2O_3 films [20–23,25–29] have been used as buried-oxide (BOX) layers. We can precisely control the thickness of the BOX layers, because the bonded SiO_2 or Al_2O_3 layers are used as BOX layers. Fig. 4a and b shows the schematic fabrication process of the InGaAs-OI substrates and a cross-sectional transmission electron microscope (TEM) micrograph of the bonded interface [23,25], respectively. The 3.2-nm-thick InGaAs-OI layer shows excellent uniformity with the smooth and abrupt interfaces. The thickness of the ultrathin BOX layer was approximately 7.7 nm. We could not find any serious damages in the extremely-thin body (ETB) InGaAs-OI layers, indicating that the developed DWB process is suitable for fabricating the high quality extremely-thin body III–V-OI on Si wafers, which is effective in suppressing SCEs. Also, the ultrathin BOX allows us to utilize the freedom of the threshold voltage control by back bias and impurity doping in Si substrates and to easily integrate III–V-OI devices with Si ones.

We have succeeded in fabricating the InGaAs-OI n-MOSFETs with InGaAs thickness of 100 nm under front-gate configuration [23,25]. The S/D regions were formed by standard Si ion implantation. Fig. 5a shows the effective mobility of InGaAs-OI MOSFETs

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