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Integration of NEMS resonators in a 65 nm CMOS technology

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ABSTRACT

In this work we study the feasibility to obtain the smallest CMOS-NEMS resonator using a sub-100 nm CMOS technology. The NEMS resonators are defined in a top-down approach using the available layers of the 65 nm CMOS technology from ST Microelectronics. A combination of dry and wet etching is developed in order to release the NEMS in an in-house post-CMOS process. Two different NEMS resonators are designed: 60 nm × 100 nm polysilicon and 90 nm × 180 nm copper clamped–clamped beams. The designed polysilicon CC Beam with a length of 1.5 μm, resonates at 232 MHz and is capable to provide the same mass sensitivity than a bottom-up silicon nanowire.

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1. Introduction

Microelectronics fabrication technologies are driving relentlessly to manufacture smaller transistors with increasing density on integrated circuit chips. The economic driving forces for this miniaturization are very strong and have driven transistor minimum feature sizes down to the 100 nm regime. In this way we can say that microelectronics technology is entering in the world of Nanotechnology.

On the other hand Nanoelectromechanical (NEMS) devices promise to revolutionize measurements of extremely small displacements and extremely weak forces, particularly at the molecular scale. NEMS can now be built with masses approaching few attograms (10^{-18} g) and with cross-sections of about 10 nm. The small mass and size of NEMS give them a number of unique attributes that offer immense potential for new applications and fundamental measurements [1].

Recently there have been some contributions which present CMOS-compatible NEMS resonators for very high performance sensing [2,3]. In these systems top-down approaches with mass production capability are used, obtaining NEMS devices with higher dimensions than CNT [4] and nanowires [5] but with very promising mass sensing capabilities. Another way to reach these minute features is to integrate new and small NEMS devices in smaller CMOS technology nodes [6]. So in order to keep on profiting the robustness of the CMOS standard process and decrease the dimensions of the top-down fabricated resonators we try to extrapolate our technological approach, previously used in AMS 0.35 μm [7] and UMC 0.18 μm [8] to ST 65 nm CMOS technology [9] where sub-100 nm dimensions can be defined.

The first consideration choosing the CMOS technology constitutes the available layers in the technology and how they affect to the resonator performance. In our particular case we will focus on its possible application as a mass sensor based on resonant beams in its first flexural mode. The mass sensitivity follows Eq. (1), where ρ is the mass density, E is the Young modulus of the material, and t and l are the thickness and length of the clamped–clamped beam respectively (see Fig. 1).

$$S_m \approx 0.74 t l^3 \rho \sqrt{\frac{\rho}{E}} \quad (1)$$

According to the last equation the best mass sensitivity will be offered by a material with the highest Young modulus and the lowest mass density (as it is shown in Table 1, being the best option carbon nanotube resonators).

Taking Table 1 into consideration, it is clear that polysilicon as a structural layer will be much better than any metal layer (aluminum or copper) available in CMOS technologies, due to its mass density Young modulus ratio, as we can see on column 3 in Table 1. In this sense we have chosen the 65 nm CMOS technology, which constitutes the last technological node in which polysilicon acts as transistor gate. In fact a polysilicon resonator with a length of 1.5 μm, 60 nm width and 100 nm thickness will reach a mass sensitivity of 66 yg/Hz at 232 MHz resonant frequency matching the experimental mass sensitivity of a bottom up silicon nanowire [5].

In contrast, this reduction of the resonator size has the disadvantage of a difficult signal transduction due to a degradation of the signal to noise ratio and the increase of parasitic and not desired effects.

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Fig. 1. Schematic of a clamped–clamped beam with symmetrical driver electrodes to allow a two port electrical characterization. Main dimensional parameters are shown.

Table 1
Cc beam mass sensitivity for different materials considering equal dimensions (l = 1 μm, t = 150 nm).

Materials	Young modulus [GPa]	Mass density [kg/m^3]	$\rho\sqrt{\frac{\rho}{E}}\ \frac{kg}{m^3}\sqrt{\frac{kg}{m^3.Pa}}$	S_m [g/Hz]
Polysilicon [10]	160	2230	0.2633	$3.121 \cdot 10^{-23}$
Aluminum [7]	131	3000	0.4540	$5.033 \cdot 10^{-22}$
Copper [11]	117	8920	2.462	$2.733 \cdot 10^{-22}$
Silicon nanowire [12]	160	2230	0.2812	$3.121 \cdot 10^{-23}$
Carbon nanotube [13]	1000	2200	0.103	$1.145 \cdot 10^{-23}$

In our previous works we have been using capacitive readout detection [14] (i.e. measurement of the current at the output driver due to the variation of the capacitance between the resonator and the electrode). This current (called motional current) can be masked if the parasitic capacitance between drivers is high enough. The ratio between them (I_m motional current and I_p parasitic current) is given by the next expression:

$$\frac{I_m}{I_p} = \frac{Z_p}{R_m} = \frac{1}{\omega C_p R_m} \tag{2}$$

where R_m is the motional resistance and can be computed as:

$$R_m = \frac{1}{Q}\frac{ks^4}{V_{DC}^2 A^2 \varepsilon^2 \omega_o} \tag{3}$$

V_{DC} is the polarization voltage, Q is the quality factor, s is the gap between resonator and electrode, k is the spring constant, A is the coupling area, ε dielectric constant and finally ω_o is the resonant frequency. The parasitic capacitance is calculated estimating the fringe capacitance between drivers [15].

A ratio of I_m/I_p = 0.31 has been measured previously [14] in the same frequency range. Fixing the clamped–clamped beam dimensions in order to obtain similar mass sensitivity than a silicon nanowire, we can check if the ratio between the motional and parasitic currents is enough to ensure the read-out. In ST 65 nm CMOS technology the metal layer (copper) with minimum dimensions is

Table 2
Main parameters for a clamped–clamped beam for different CMOS technologies (see Fig. 1 for dimensions). In order to calculate R_m a V_{DC} of 20 V has been applied in AMS Technology meanwhile a V_{DC} of 30 V has been assumed to ST cases due to its higher snap-in voltages).

	l (μm)	w (nm)	t (nm)	s (nm)	l_D (μm)	w_D (μm)	f_o (MHz)	R_m Q = 300 (air)	C_p (aF)	S_m (g/Hz)	I_m/I_p
AMS	3.5	350	282	150	3.2	5.0	243	31.1 MΩ	61.5	$2.51 \cdot 10^{-21}$	0.34
ST Poly	1.5	60	100	180	1.14	2.44	232	24.7 MΩ	13.9	$6.6 \cdot 10^{-23}$	1.99
ST M1	1.17	90	180	160	0.81	2.46	245	69.5 MΩ	18.9	$56.8 \cdot 10^{-22}$	0.49

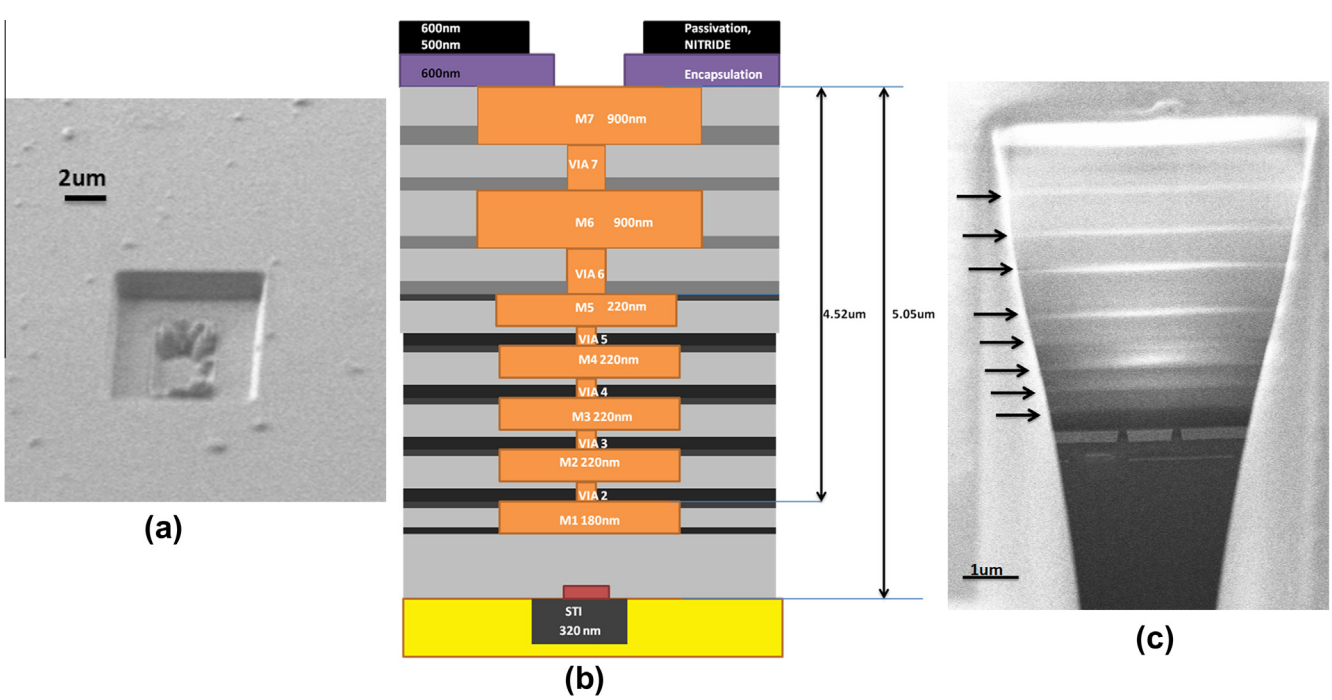

Fig. 2. (a) SEM image of the resonator area as received from the ST CMOS technology foundry. (b) Cross section schematic of ST 65 nm technology showing the WINDOW, that is defined on the ENCAPSULATION and PASSIVATION layer in order to release the structure. (c) SEM image of a Field Ion Beam cut of the CHIP over a metal M1 resonator area as it is received from the foundry. The different silicon oxide and etch stopper layers are clearly appreciated and are indicated with an arrow.

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