

Optimum bias of power transistor in 0.18 μm CMOS technology for Bluetooth application

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Abstract

Based on the proposed silicon integrated power transistor adopting a 0.18 μm technology, its performance shows this novel device can be operated at 2.4 GHz for Bluetooth and lithium battery applications [Hsu H-M, Su J-G, Chen C-W, Tang DD, Chen CH, Sun JY-C. Integrated power transistor in 0.18 μm CMOS technology for RF system-on-chip applications. *IEEE Trans Microwave Theory Tech* 2002;50(December):2873–81]. After executing matrix measurement of large-signal characteristics, the optimal quiescent point can be found, and the associated large-signal performance exhibits a maximum output power with 21.26 dBm, corresponding to a value of 44.3% for power added efficiency (PAE). Therefore, this device can be used in handholds for short-distance, low-power, and high-frequency operation.

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1. Introduction

The rapid evolution of advanced digital signal processing (DSP) and RF communications has evolved from traditional radio and television broadcasting to a broad spectrum of exciting applications, such as cellular systems, smart handheld devices, wireless LANs [2], Bluetooth [3], home RF, global positioning system (GPS), and broadband satellite solutions. These applications for communication of voice, data, and video anywhere at any time rely on advances in semiconductor IC technologies to provide integrated solutions at affordable cost.

The advances in microelectronics have been a determining factor in this evolution. Submicron process technologies have resulted in DSP chips with more computing

ability. The RF front end has shifted from discrete components to a solution with only a few ICs. Intense research is devoted to investigating possibilities of integrating the complete front end on a single chip [4,5]. This should enable products with large reduction in volume, mass, cost, and power consumption.

Because of the progressive development in CMOS technology for VLSI applications, the channel length has been shrunk into deep submicron dimension. The advantage of deep submicron CMOS technologies is that the cut-off frequency (f_T) of NMOS devices is getting close to that of bipolar transistors. It can achieve approximately 70 GHz in 0.18 μm CMOS technology, as demonstrated for mass production in this paper [6]. The excellent characteristics give sufficient frequency performance for analog signal processing at 1–5 GHz; hence, a powerful digital baseband signal-processing core can be added on the same chip.

Integrated power transistors for 2.4 GHz application by 0.18 μm CMOS technology were successfully demonstrated in previous literature [1]. In this study, an effort is dedicated

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to characterize the large-signal performances of this power transistor. A matrix measurement of 20 points is performed to find the optimum bias needed to satisfy the specifications of Bluetooth with operation at 2.4 GHz and 20 dBm of output power on lithium battery supply.

2. Device performances of power transistor

Silicon integrated power transistor by 0.18 μm CMOS technology was successfully implemented in a previous study [1]. The cross-section of MOS transistor for high-power application is depicted in Fig. 1. One additional mask for N-implantation surrounding the drain side is adopted to decrease the concentration near the drain side; hence, the gradient of the concentration is reduced in this region. Since a high-voltage is forced on the drain terminal, which suffers a strongly electric field during operation of the device. The smooth decrease of the concentration alleviates the electric field on the drain side and results in an improvement of the breakdown voltage. Based on reported results, the drain current and voltage with various gate biases are illustrated in Fig. 2. It shows the device can be operated at least to 10 V by sweeping the gate voltage from 0 V to 3.3 V.

RF small-signal characterization is paramount due to the trade-off between DC bias and RF performance during

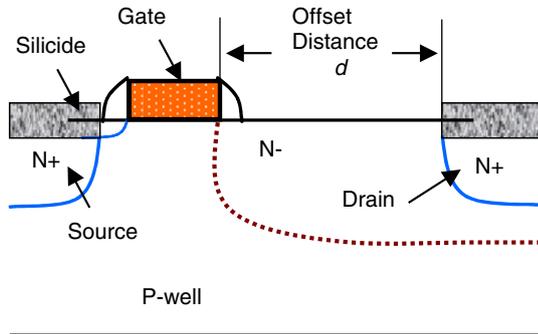


Fig. 1. Cross-section of integrated power transistor.

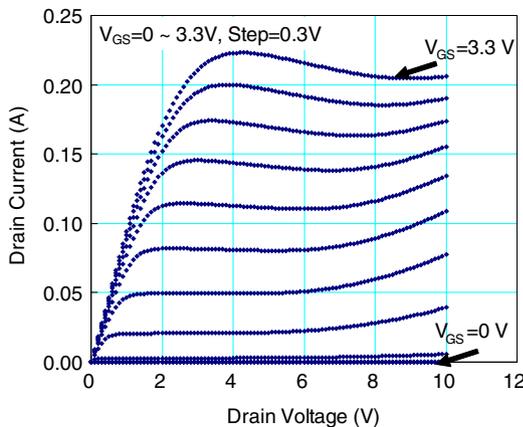


Fig. 2. Plots of DC characteristics for integrated power transistor.

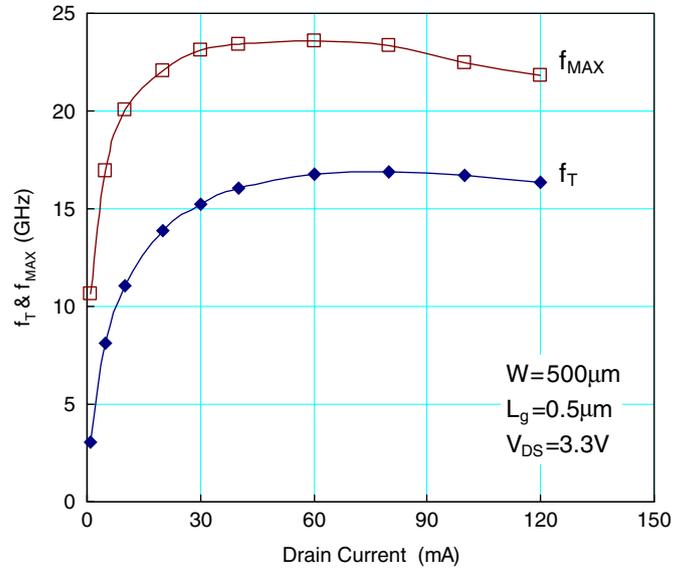


Fig. 3. Plots for cut-off frequency (f_T) and maximum oscillation frequency (f_{MAX}) of integrated power transistor.

device operation [7]. Therefore, RF small-signal behavior was measured to understand the upper frequency limitation of device operation. For RF small-signal performance, the MOS transistor is biased at a gate voltage with maximum gate transconductance and a drain bias equal to 3.3 V. The values of f_T and f_{MAX} are extracted from obtained S-parameters in high-frequency measurements with an Agilent 8510 C network analyzer and a Suss probe station. All on-wafer measured S-parameters were taken with a de-embedding procedure to remove undesired pads parasitics [8].

Fig. 3 depicts the cut-off and maximum oscillation frequencies achieving to 16 GHz and 24 GHz, respectively. Hence, the device is more than enough to operate at 2.4 GHz for wireless applications. That the DC voltage can be operated at least to 10 V means that the designed device is suitable for lithium battery operation. Therefore, this power transistor has great potential applications for portable products with wireless communication.

3. Characterizations of large-signal performances

Based on the results in last section, large-signal performance, such as output power, power added efficiency (PAE), power gain and 1 dB gain compression point, is characterized at 2.4 GHz to investigate device behavior. The quiescent bias is essential for large-signal operation since it affects the output power and corresponding efficiency. Generally, the overdrive of drain voltage can enhance output power, but an increase of the quiescent current will move the bias point from class-AB to class-A and degrades efficiency.

Therefore, a matrix measurement of power characteristics is performed in order to obtain the optimum operation by considering both RF output power greater than 20 dBm

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