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Crosstalk effects in mixed-signal ICs in deep submicron digital CMOS technology

V. Liberali*, R. Rossi, G. Torelli

Department of Electronics, University of Pavia, Via Ferrata 1, 27100 Pavia, Italy

Abstract

This paper illustrates the crosstalk phenomenon and its impact on the design of mixed analog/digital circuits with high accuracy specifications. Generation of digital disturbs, propagation through the substrate, and effects on analog devices are considered, with particular emphasis on integrated circuits realized on heavily doped substrate, where traditional shielding is less effective. Techniques to reduce analog/digital crosstalk are reviewed and discussed. A simple modeling approach is presented, suitable for the analysis of crosstalk effects using a conventional electrical simulator (SPICE). Experimental results on a test chip are presented to validate the modeling approach. © 2000 Elsevier Science Ltd. All rights reserved.

Keywords: Analog/digital circuits; Crosstalk phenomenon; Modeling approach

1. Introduction

Microelectronics industry is geared toward an ever-expanding use of digital circuits, because digital data is easy to process and store and digital design can take immediate advantage of technology scaling down. In the past 30 years, MOS device size reduction has led to an exponential growth in integration density, with a 1.35–1.5 increase factor per year: this trend known as "Moore's law" [1,2], is the main driving force of timing schedule for the semiconductor industry [3]. Fig. 1 illustrates the forecasted reduction of CMOS minimum gate length during next years. The corresponding integration density increase (in millions of transistors per square centimeter) is plotted in Fig. 2.

Important consequences of technology scaling are the increase in the computational power of CMOS digital processors, the fabrication of single-chip integrated systems, and the migration to CMOS technology of a wide variety of integrated circuit applications, whenever possible.

However, being the real world steadily analog, interfaces between the digital processor and external variables must be used. This leads to the need for analog-to-digital (A/D) and digital-to-analog (D/A) converters, and, in some cases, analog pre-processing and/or signal conditioning. Such functions should be integrated together with the digital circuitry onto the same silicon chip.

Microintegrated technology for mixed analog/digital circuits usually is one generation behind the most advanced pure digital technology. Nowadays, mixed analog/digital circuits are developed in 0.25 μm CMOS, while state-of-the-art digital integrated circuits (ICs) are in 0.18 μm CMOS technology. Experiments of CMOS integration in sub-0.1 μm technology have also been carried out. Transistors with a gate length of 50 nm have been fabricated, and theoretical studies prove that ultra-small geometry MOS devices are possible, with a gate length in the order of 20 nm or below [4].

Such a technological trend will enable CMOS circuits for digital signal processing (DSP) to be developed for a broad variety of applications. Market trend is towards integration of home-based services and hand-held electronic products [2]. Communication systems are playing the leading role, offering new broad-band services, either wireless or wire-based [5]. Two emerging examples are data transmission over twisted pairs (asymmetrical digital subscriber loop or ADSL) [6–8] and radio-frequency (RF) portable communication systems [9]. In the near future, digital video systems are expected to provide opportunity for new value-added services: high-definition TV, video-on-demand, and virtual reality applications will become more and more important as soon as technology improvement will allow transmission of video signals over existing links [10].

Low-cost and high-performance circuits are required to be competitive in a more and more demanding consumer

* Corresponding author. Tel.: +39-382-505-226; fax: +39-382-422-583.
E-mail addresses: v.liberali@ele.unipv.it (V. Liberali), r.rossi@ele.unipv.it (R. Rossi), g.torelli@ele.unipv.it (G. Torelli).

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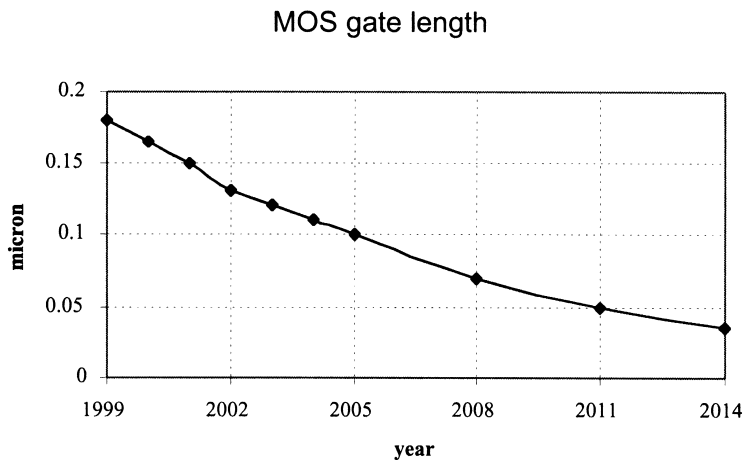

Fig. 1. Minimum CMOS gate length forecast.

market. Single chip solutions [11] reduce costs and increase reliability. Moreover, they can help to reduce weight and size of hand-held electronic products (although a large part of the volume is dedicated to the batteries).

In mixed systems, performance limitations come mainly from the analog section which interfaces the digital processing core with the external world. In addition to the difficult task of designing state-of-the-art analog/digital interfaces, mixed analog/digital microintegrated circuits offer an additional challenging aspect. In such ICs, coupling from switching digital nodes and power supplies to analog devices through the common substrate is a serious limitation to analog circuit performance.

As an example, an ADSL interface needs a 12-bit analog/digital section operated at 4 MHz clock rate. This application requires a careful control of analog/digital crosstalk [12].

Reduction of effects coming from digital noise can be achieved in four different ways: (i) by reducing the disturb injected into the substrate by means of a low-power digital design; (ii) by inserting shields between analog and digital sections, to attenuate the injected noise; (iii) by designing analog structures which are insensitive to digital noise; and (iv) by using suitable assembling techniques. These items will be considered in the following sections of the paper. Moreover, this paper will discuss some techniques for computer simulation of noise generation and propagation in high density ICs. Finally, some experimental results on a test chip designed to characterize crosstalk mechanisms will be presented.

2. Technology

Technology development is driven by market demand. Main targets are lower cost, high performance, and high integration density [13].

Modern CMOS technologies use a heavily doped substrate (p^+) covered by a lightly doped epitaxial (epi) layer of the same polarity (p). The epi layer is very thin

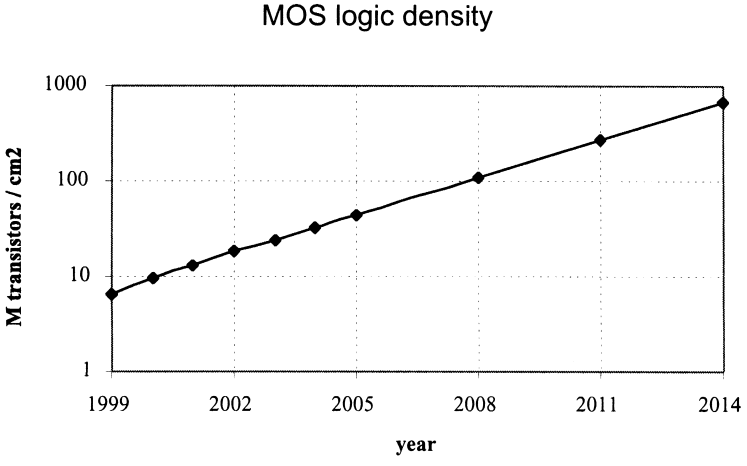

Fig. 2. CMOS gate density forecast.