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The Ge condensation technique: A solution for planar SOI/GeOI co-integration for advanced CMOS technologies?

B. Vincent [a,*], J.F. Damlencourt [a], Y. Morand [b], A. Pouydebasque [a], C. Le Royer [a], L. Clavelier [a], N. Dechoux [b], P. Rivallin [a], T. Nguyen [c], S. Cristoloveanu [c], Y. Campidelli [b], D. Rouchon [a], M. Mermoux [d], S. Deleonibus [a], D. Bensahel [b], T. Billon [a]

[a] CEA-LETI Minatec, 17 rue des Martyrs, 38054 Grenoble Cedex 9, France
[b] STMicroelectronics, 350 Avenue J. Monnet, 38926 Crolles Cedex, France
[c] IMEP, INP Grenoble-Minatec, BP 257, 38016 Grenoble Cedex 1, France
[d] LEPMI/ENSEEG/INPG, 1130 Rue de la Piscine, 38402 St Martin d'Hères, France

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ABSTRACT

This paper presents a general study on the germanium (Ge) condensation technique to assess its potential, issues and applications for advanced metal oxide semiconductor field effect transistor (MOSFET) technologies. The interest in such process for fabrication of ultrathin germanium on insulator (GeOI) layers for fully depleted GeOI MOSFETs application is first described. We highlight the impact of initial silicon on insulator (SOI) substrates uniformity on the process, determined as the key parameter to be improved. Next, a global procedure is described for MOSFETs integration on Ge layers grown on 75% Ge-enriched silicon germanium on insulator (SGOI) substrates obtained by the Ge condensation technique. A third section reviews the different local Ge condensation techniques for fabrication of SOI–GeOI hybrid substrates. Interests of such substrates for SOI–GeOI planar co-integration either at the microprocessor, at the cell or at the transistor level will be discussed. Finally, the fabrication of a first 50-nm-thick SOI–GeOI hybrid substrate is described.

0. Introduction

Since the fabrication of the first metal oxide semiconductor field effect transistor (MOSFET) in 1960 based on silicon/silicon dioxide tandem, the microelectronics research and industry have been driven by scaling down all transistor dimensions. Scaling enabled and still permits improvements at the transistor level (enhancement of ON current, I_{ON}), at the circuit level (reduction of circuits delay, τ_t), and also responds to the economical constraint of enhancing continuously the transistors density on Si wafers. The end of scaling is however approaching [1]: technical limitations will indeed impede infinite shrinkage. New technologies are then emerging to overcome scaling issues and continue improvements at the transistor and circuit levels: channel mobility/velocity enhancement, like gate length scaling, induces both I_{ON} increase and τ_t reduction. Three pathways are detailed in the literature to enhance the carrier mobility and velocity within the channel: alternative channel orientations, strain implementation, and Si replacement by high mobility materials such as germanium or III–V alloys [2].

In particular, silicon germanium on insulator (SGOI) or germanium on insulator (GeOI) substrates appears to be highly interesting structures for advanced CMOS technology. Such layers may be first used as efficient channel materials [3] combining benefits from both Ge material

* Corresponding author at: IMEC, Kapeldreef 75, 3001 Leuven, Belgium.
E-mail address: benjamin.vincent@imec.be (B. Vincent).

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(high mobility/velocity, longer energy relaxation time and same crystal structure as silicon) and "On Insulator" technology (better electrostatic control of the gate, reduced junction capacitance and lower substrate coupling in radio frequency). Moreover, SGOI layers with high Ge contents may be used as template materials for various advanced semiconductors as tensely stained Si layers, compressively strained Ge layers, or III–V alloys [4].

Many techniques have been reviewed to develop SGOI or GeOI layers, as wafer bonding, bond and etch back technique, rapid melt growth, or Ge condensation method [5]. The latter technique, proposed by Tezuka in 2001 [6,7], is based on a selective Si oxidation of a $Si_{1-x_i}Ge_{x_i}$ layer grown on a silicon on insulator (SOI) substrate with an initial low Ge content, x_i. During oxidation, Ge atoms diffuse through SiGe and top Si layers forming a SGOI layer; the oxidized and BOX layers act as Ge diffusion barriers. The remaining SGOI layer is thinned during the Si selective oxidation which results in a Ge-enriched film.

Compared to its rival techniques, the main advantage of the Ge condensation process is the seeming easiness to carry out local SGOI or GeOI structures on SOI wafers at either the microprocessor level, cell level or transistor level.

For instance, whereas Ge is characterized as a high mobility material, its small bandgap (compared to Si) induces unfortunately important leakage currents: Ge presence within advanced microprocessors could then be only restricted to local blocks where high-speed performance is required whereas Si material is kept within the rest of the microprocessor, where leakage currents are detrimental.

At a smaller scale, at the cell level, local GeOI or SGOI active zones on SOI substrates are also interesting for co-integration of planar n- and p-MOSFETs, respectively, on SOI and GeOI structures. At present, whereas Ge electron and hole mobility are theoretically higher than Si ones, no improvements for n-MOSFETs on GeOI substrates have been shown in the literature yet. To our knowledge, benefits of Ge for electron mobility enhancement have only been described by simulation [8,9] or experimentally with Ge grown layers on Si substrates [10]. On the contrary, p-MOSFETs fabricated on 93% Ge-enriched SGOI substrates (1.3% compressively strained) have already shown a peak hole mobility equal to 1593 $cm^2/V s$, i.e. exhibiting a $10\times$ enhancement compared to the Si universal hole mobility [11]. If GeOI, or highly enriched SGOI layers are not confirmed in the future as efficient substrates for n-MOSFETs, use of Ge could be only restricted to p-MOSFETs and then SOI–GeOI hybrid substrates fabrication would be the useful solution.

At an even smaller scale, at the transistor level, restriction of Ge only within transistor channels on active zones is an interesting approach. Ge-channel MOSFETs with Si source and drain, compared with plain Ge MOSFETs may offer large OFF currents reduction [2]. A unique channel Ge-enrichment method was proposed by Tezuka [12]. We note that SOI/SGOI or SOI/GeOI hybrid substrates can only be obtained by local Ge condensation techniques whatever the co-integration scale.

This paper presents a general study on the Ge condensation process. We first present a review of previous published works to assess the technique for elaboration of 200 mm SGOI substrates. Description of critical issues will let us conclude that Ge condensation technique should be better used for mid-Ge-enriched (25–75%) SGOI layers fabrication. Next, the use of such mid-Ge-enriched SGOI layers obtained by Ge condensation as buffer substrate for Ge layers growth and subsequent device integration is detailed in a second part. Then, a third section focuses on the fabrication of hybrid SOI–GeOI substrates. Different local Ge condensation techniques are reviewed and the first fabrication of a 50-nm-thick hybrid substrate is presented. Finally, a discussion is proposed to clearly define applications of the Ge condensation process in advanced CMOS technology.

1. Status of the Ge condensation technique for 200 mm SGOI wafers

The first initial structure proposed for the Ge condensation technique was a low Ge content SGOI layer previously obtained by the SIMOX method [6]. A selective Si oxidation of the SGOI layer was next performed to allow Ge enrichment. Shortly, another starting substrate was proposed by growing low Ge content $Si_{1-x_i}Ge_{x_i}$ layers on SOI wafers [7] as initial SGOI structures. The development of such $Si_{1-x_i}Ge_{x_i}$/SOI substrate, usually named pre-structure, is even more pertinent when the $Si_{1-x_i}Ge_{x_i}$ layer is compressively strained because it avoids the presence of misfit dislocations within this initial stack. $Si_{1-x_i}Ge_{x_i}$ grown layers are thinner than the critical thickness of plastic relaxation. Since the critical thickness decreases with Ge content, the Ge amount within the pre-structure is limited. In advanced Ge condensation processes [13,14], Ge amount is conserved during the whole Ge enrichment of the SGOI layer: final SGOI layers with high Ge contents are then necessarily ultra-thin (about 10 nm). In the following, we will review previous published results in order to assess the potential of the Ge condensation technique for elaboration of 200 mm SGOI wafers.

The first issue concerns defects generation. We demonstrated by experiment and calculation the existence of a threshold Ge-enrichment value above which strain relaxation occurs via stacking faults generation [15]. Starting with different conventional pre-structures (different initial SiGe thickness and Ge content), the threshold value never exceeds 82%: in other words, whatever the initial parameters, defect-free SGOI layers with Ge contents higher than 82% cannot be obtained. This conclusion is contradictory with the initial description from Tezuka et al. in 2001 who claimed that strain relaxation during the Ge condensation technique can be assisted by BOX viscous flow which then impedes any dislocation formation. The latter hypothesis is not fully satisfactory: high Ge enrichments impose lower oxidation temperatures than the SiO_2 viscous temperature, equal to 960 °C [16], in order to avoid any SiGe-enriched melting. Recently, Nakaharai et al. [17] indeed confirmed that microtwins are necessarily formed during Ge condensation technique by strain relaxation.