Available online at www.sciencedirect.com
SCIENCE DIRECT®
Microelectronic Engineering 70 (2003) 144–157
MICROELECTRONIC ENGINEERING
www.elsevier.com/locate/mee

Towards implementation of a nickel silicide process for CMOS technologies

C. Lavoie*, F.M. d'Heurle, C. Detavernier, C. Cabral Jr.
IBM T.J. Watson Research Center, 1101 Kitchawan Road, Yorktown Heights, NY 10598, USA

Abstract

In this paper, we review some of the advantages and disadvantages of nickel silicide as a material for the electrical contacts to the source, drain and gate of current and future CMOS devices. We first present some of the limitations imposed on the current cobalt silicide process because of the constant scaling, of the introduction of new substrate geometries (i.e. thin silicon on insulator) and of the modifications to the substrate material (i.e. SiGe). We then discuss the advantages of NiSi and for each of the $CoSi_2$ limitations, we point out why Ni is believed to be superior from the point of view of material properties, miscibility of phases and formation mechanisms. Discussion follows on the expected limitations of NiSi and some of the possible solutions to palliate these limitations.

Keywords: Nickel silicide; NiSi; Diffusion; Metal rich phase; Agglomeration; Film stability; $CoSi_2$

1. Introduction

The reaction of Ni and Si for possible use in microelectronic manufacturing has been extensively studied starting in the mid 1970s [1–13]. In the last 3–5 years, the interest in the low resistivity NiSi increased significantly because of the foreseeable use as contact to the source, drain and gates of CMOS devices. Microelectronic companies have recently published results on NiSi contacts [14–27] pointing out that the advantages of this material reside in a low thermal budget for formation, a low resistivity in narrow dimensions and a low device leakage. While these device data have shown the feasibility of a NiSi process, the actual use of this new material depends to a great extent on the performance and limitations of the current $CoSi_2$ contacts as well as on improvements in yield for the NiSi process. As many properties of NiSi are very different from those of its $CoSi_2$ counterpart, a good understanding of the advantages and limitations of each material is required before the use of NiSi in devices becomes a reality.

2. Limitations of $CoSi_2$

As the production of transistors reaches gate lengths significantly shorter than 50 nm, the formation of cobalt silicide contacts becomes more difficult. There are three main factors that limit the extendibility of this material in future devices:

1. The rise in resistance in very narrow lines
2. The reduction in available Si for the reaction as the silicon-on-insulator substrates become very thin

*Corresponding author. Tel.: +1-914-945-2180; fax: +1-914-945-2141.
E-mail address: clavoie@us.ibm.com (C. Lavoie).

0167-9317/03/$ – see front matter
doi:10.1016/S0167-9317(03)00380-0

3. The introduction of SiGe substrates

The first concern is reminiscent of the problem that was faced in the 1990s with $TiSi_2$. In this case, the low nucleation density of the desired C54 $TiSi_2$ phase was at the origin of a resistance increase in lines narrower than 350 nm [28,29]. While the nucleation density could be increased with the addition of transition elements and allow for low resistance contacts down to about 200 nm [30], the further decrease in gate lengths required the introduction of $CoSi_2$ contacts. This low resistivity material did not show formation problems in the smallest achievable dimensions at the time of implementation (~100 nm). Recent work [18,20,24] shows, however, that the resistance of $CoSi_2$ lines increases dramatically with a further decrease in line width. The line width at which the resistance increases depends on the process itself and the test site (line length and geometry) and has been reported to be linked with the presence of infrequent voids in narrow silicide lines. The origin of these voids is not clear and may depend on the presence of impurities, on early and non uniform agglomeration in smaller dimensions, on local stresses, or even on the mechanism of formation (diffusion or nucleation controlled/diffusing species). Most likely, we are here in the presence of a combination of these factors. While this first concern with the continued use of $CoSi_2$ can be alleviated through optimization of the material itself [31], the following additional limitations are not avoidable when using a standard Co self aligned silicide process.

The second factor limiting $CoSi_2$ is the use of thin silicon on insulator (SOI) substrates. The sheet resistance requirements for contacts to current devices are such that the thickness of $CoSi_2$ must be in the range of 20 to 30 nm. From the crystal structures and atomic volumes, one easily determines that the consumption of Si necessary to form this low resistivity layer is 3% thicker than the silicide itself. (It is interesting to note that the density of Si atoms in $CoSi_2$ is higher than in Si itself). To the silicide layer thickness, one must also add the peak to peak roughness of the interface. Indeed, the interface $CoSi_2$/Si is inherently rough because of the nucleation controlled formation of $CoSi_2$ from CoSi. While this roughness can be controlled through optimized cleaning procedure and alloying [31,32], it cannot be eliminated and the typical maximum layer thickness can locally be 20–30% larger than the average $CoSi_2$ thickness. When the thickness of the SOI layer reaches about 40 nm, at least part of the silicide film will touch the underlying oxide layer causing degradation in contact resistance and device properties.

The last factor restricting the $CoSi_2$ extendibility is the modification of the substrate material with Ge, introduced into the Si to modify the stress in the substrate layer and thereby enhance the carrier mobility and increase the device switching speed. The formation of $CoSi_2$ in the presence of Ge is extremely arduous [31,33,34]. Germanium is soluble in CoSi and immiscible in $CoSi_2$. As a result, the formation of $CoSi_2$ from CoSi requires that the Ge be expelled from a growing $CoSi_2$ grain. From in situ measurement of phase formation, we have determined that not only the growth of the phase is retarded but its nucleation is also elevated to much higher temperatures. From classical nucleation theory [35], it can be shown that the change in entropy of mixing from a solution to a mix of phases raises the barrier for nucleation [31,34–36]. For manufacturing, this results in an increase in the nucleation of $CoSi_2$ from about 600 °C to above 800 °C. This processing temperature is too high with respect to the manufacturing of advanced devices but also for the integrity of the silicide itself. The presence of the low melting point Ge in the film reduces the agglomeration temperature to the point where the process window between the silicide formation and agglomeration becomes non existent.

While these concerns can be alleviated with the selective addition of epitaxial Si to the source and drain of transistors (raised source/drain process), the possibility of implementation of a NiSi process is interesting both in terms of the cost and process complexity limitations.

3. Advantages of NiSi

The front up candidate for the replacement of $CoSi_2$ shows improved performance with respect to the three limitations presented above. The main advantages of NiSi can be separated in the four categories listed below:

1. Reduced thermal budget