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ScienceDirect
Sensors and Actuators A 145–146 (2008) 207–213
SENSORS AND ACTUATORS A PHYSICAL
www.elsevier.com/locate/sna

Silicon nanowire sensor array using top–down CMOS technology

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Received 19 June 2007; received in revised form 20 November 2007; accepted 9 December 2007
Available online 28 December 2007

Abstract

The paper elaborates the silicon nanowire (SiNW) arrays fabrication using standard CMOS compatible technologies (top–down) with each array consisting of 100 wires, which are individually electrically measurable for their conductance and facilitating statistical analysis. To facilitate real-time analysis, the arrays are integrated with micro-fluidics for the delivery of various chemicals for surface modification, buffer solutions, bio-molecules/analytes, etc. The silicon nanowires are also presented as nano-temperature sensors in two configurations, i.e. as resistance temperature detector (RTD) and diode temperature detector (DTD) types. RTD type sensors have shown temperature coefficient of resistance (TCR) values ~7500 ppm/K which are enhanced beyond 10,000 ppm/K by the application of back-bias. DTD type sensors using nanowires have recorded more than one order variation in reverse-bias current, in the temperature range of 293–373 K. Both the types of nano-temperature sensors are highly sensitive and can be integrated with other bio-chemical sensors in lab-on-chip devices. Nanowire array fabrication details in particular as nano-temperature sensor are elaborated here along with their characterization.

Keywords: Silicon nanowires; CMOS compatible; Nano-temperature sensor; Field effect transistors (FET)

1. Introduction

Uni-dimensional silicon nanowires (NW) [1], carbon nanotubes (CNT) [2], SnO_2 and In_2O_3 nanowires [3,4], are being explored for biological and chemical sensors because of their high surface/volume ratio [5]. Various nano-sized temperature sensors using carbon nanotubes [6–9] and focused ion chemical vapor deposition of tungsten over atomic force microscope (AFM) cantilevers [7] are also reported. The bio-chemical sensing mechanism is understood as change in surface charges of nanostructures with the presence of molecular species, which modulates the conductance of the nanowire [2]; the devices are analogous to biologically gated field effect transistors (FET). The silicon nanowire (SiNW) are accredited as temperature sensor because of the fact that the conductance of these semiconductor wires is highly dependent on temperature. Also, most of the techniques reported for nano-temperature sensor face mass fabrication challenges like assembly of CNT as thermal probe, recording gallium meniscus as function of temperature with the help of scanning electron microscope or precursor gas adsorption on the AFM cantilever tip. The mass manufacturing with reproducibility and integration with other functionalities in a biochip is extremely challenging for these sensors.

It is important to develop technologies that can reliably produce silicon nanowires. We demonstrate the fabrication of silicon/poly-silicon nanowire arrays using standard CMOS technology (top–down) with each array consisting of 100 wires, which are individually electrically measurable for their conductance and facilitating statistical analysis. The arrays are integrated with micro-fluidics for delivering the bio-molecular solutions. Our approach paves way for realizing high-density, highly sensitive bio-chemical sensor chips integrated with nano-temperature sensors using mass fabrication technologies and thus has the potential to achieve multiplexed diagnosis which is essential for understanding and curing of complex diseases. The approach also has the inherent advantage of integrating with Si-based signal processing and communication circuits.

2. Process details

2.1. Nanowire array fabrication

Silicon nanowires are realized on 8″ diameter wafers. For single crystal silicon nanowires, silicon-on-insulator (SOI) wafers with ~50 nm buried oxide and 80 nm device silicon layers are

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0924-4247/$ – see front matter
doi:10.1016/j.sna.2007.12.019

Nanowire (NW) array fabrication

- SOI wafer or poly-silicon on oxidized silicon wafer/ NW implantation
- Si fin pattern (DUV lithography)
- Reactive ion etching/ Photo resist strip/ Wet clean
- Dry oxidation (2-6hrs) to form nanowires
- Source-Drain (S/D) implantation
- Pre-metal dielectric deposition and S/D Contact etch
- Contact metal deposition/ patterning
- Si_3N_4 passivation deposition
- Contact pad open
- Dielectric etch in nanowire area
- Alloy

Micro-fluidic channel fabrication

- Silicon nanowire array
- Channel definition using SU8 resist (~40μm)
- Hard baking
- NW surface cleaning and modification (optional)
- Channel capping with glass plates\ PDMS having fluidic Input/ Output ports
- Thermo-compression

Fig. 1. Process flow for the fabrication of silicon nanowire array and micro-fluidic channels.

used. And for poly-silicon nanowires, 80 nm thick poly-silicon is deposited on 50 nm thick thermal oxide grown on p-type test wafer. The wafers are then doped with p-type (boron) or n-type (phosphorous) impurities using an ion implanter where implant dose is varied from 1×10^{13} to 1×10^{15} and energy from 30 to 50 keV. The dopants are then activated in rapid thermal annealing furnace and nanowire-fins are patterned (using standard DUV lithography) in the array format; silicon/poly-silicon is etched in reactive ion etcher and resulting fins (60–80 nm wide) are oxidized in O_2 at 900 °C (for 2–6 h) to realize nanowire array. The two ends of the nanowires are further doped to obtain n+ or p+ regions, followed by connecting to contact metal and alloying to realize Ohmic contacts. The device is then passivated by silicon nitride film except for the active nanowire sensor area and metal pads. Process flow for the fabrication of silicon nanowire array is depicted in Fig. 1.

Resistance temperature detector (RTD) and diode temperature detector (DTD) are fabricated with the identical fabrication processes except for the different implant patterns. Diode-type temperature detectors were realized by selectively doping the n- and p-regions of the nanowires, using lithography. Similarly, the two contacts were doped to form n+ and p+ contact areas. Schematic top view of nanowire DTD and RTD, showing the implantation types and locations are shown in Fig. 2. Nanowires being the integral part of the various micro-fluidic devices consisting of NW-based bio-chemical sensors in array format, certain NW devices can be designated for temperature sensing while others for diagnostics.

2.2. Micro-fluidic channels fabrication

Micro-fluidic channels are realized on the passivated silicon nanowire array wafers using SU-8 photo resist, a wafer-level process. The channel depth up to 40 μm are realized, which are capped by polydimethyl-siloxane (PDMS) or glass slides using thermal compression at low temperatures (<60 °C). The fluidic input and output ports are also integrated in the PDMS or glass caps. The process flow for the fabrication of micro-fluidic channels on the nanowire array chips is also depicted in Fig. 1.

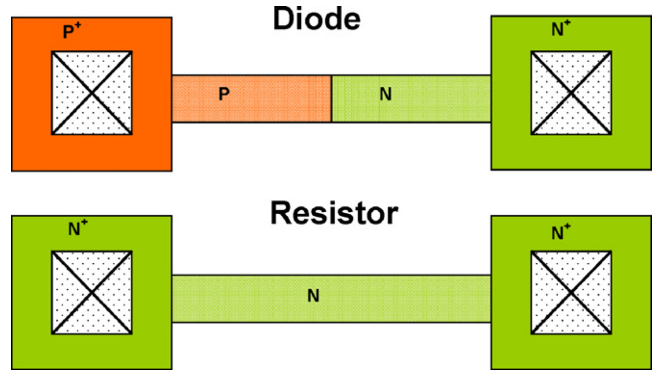

Fig. 2. Schematic top view of nanowire diode and resistor, showing the implantation types and locations. Crossed areas are the contact windows for metal lines.

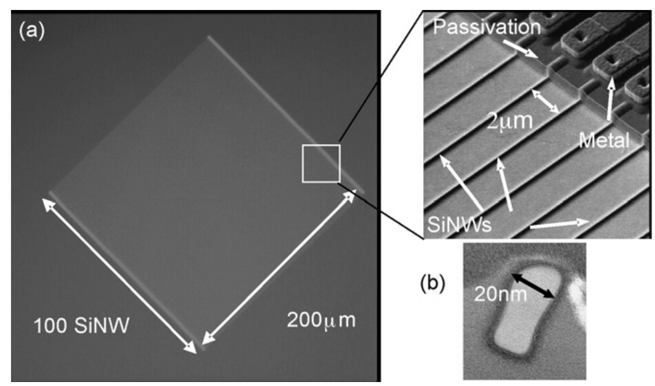

Fig. 3. (a) Optical image of 200 μm long nanowire array showing 100 wires; zoom-in SEM image shows nanowires spaced at 2 μm with metal lines and passivation layer. (b) TEM image of nanowire showing rectangular cross-section.

An optical image of 200 μm long nanowire array having 100 nanowires is shown in Fig. 3(a) while zoom-in SEM image shows nanowires pitched at 2 μm, contact metal lines and passivation layer. A typical TEM image of a nanowire in Fig. 3(b) suggests rectangular cross-section of the nanowire with 20 nm width and 40 nm height. However, the nanowires with different cross-sectional dimensions and shape (rectangular, triangular or circular) are obtained by controlling Si-fin width, height and oxidation time as reported earlier [10]. A sensor chip having two arrays of 200 μm long nanowires (100 NW in each) with 40 μm deep fluidic channels in SU-8 (uncapped) is depicted in Fig. 4. Zoomed-in image shows the fluidic channel across nanowire array with circular I/O port at one end.

3. Results and discussions

3.1. Electrical characterization of the nanowire arrays

The electrical conductance of nanowire sensors is measured using semiconductor wafer prober along with parametric analyser. The conductance is calculated as the mean of data points recorded while potential across the sensor is scanned from −0.5