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Design and implementation of a capacitive fingerprint sensor circuit in CMOS technology

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Abstract

An ASIC implementation of capacitive fingerprint sensor is described for user authentication on small, thin, and portable equipment. New charge sharing sensing circuit minimizes the influence of internal parasitic capacitances and enlarges the voltage difference between a ridge and valley. A voltage comparator can easily discriminate a ridge and valley. Our method results in about 180% improvement in the voltage difference between a ridge and valley. The sensing circuit also includes a pixel-level automatic calibration scheme. The proposed calibration scheme initializes a capacitive fingerprint sensor LSI to eliminate the influence of the surface condition and environment, which is degraded by dirt during long-time use. The test chip is fabricated on a 0.35 μm standard CMOS 1-poly 4-metal process.

Keywords: Fingerprint sensor; Capacitive; Pixel array; Charge sharing; Image algorithm; Pixel-level automatic calibration scheme

1. Introduction

Recently, some small, thin, and inexpensive direct-touch capacitive semiconductor fingerprint sensors have been proposed [1–5]. A capacitive fingerprint sensor uses a capacitive sensor array to detect fingerprints. The name ‘capacitive’ comes from the fact that the finger skin and the sensor electrode produce a capacitor whose capacitance is determined by the distance from the chip surface to the finger skin.

The conceptual model of a capacitive sensing scheme is shown in Fig. 1. The finger is modeled as the upper electrode of the capacitor, and the metal plate in the sensor cell as the lower electrode. These two electrodes are separated by the passivation layer of the silicon chip and air. C_{ox} has a fixed capacitance which is determined by the passivation-layer thickness d_{ox} and the relative dielectric constant ε_{ox}. C_{air}, however, has a variable capacitance according to the distance d_{air}. The series-connected capacitor C_f is composed of a capacitor between the metal plate and the chip surface and another one between the chip surface and the finger skin. The capacitance of C_f is at its maximum value when a ridge has contact with the passivation layer. As the distance between the chip surface and the finger's skin increases, the capacitance becomes smaller. The variation of capacitance is transferred to output voltage by sensing scheme. The comparator discriminates a ridge and valley by reference voltage as shown in Fig. 1(b).

One of the most important performances of a capacitive sensor is its sensitivity because the capacitance to be detected is of the order of femtofarads. Sample and hold scheme [4], feedback capacitive sensing scheme [5], charge transfer scheme [3] and charge sharing scheme [1] have been designed to detect the weak sensor signal. This paper analyzes the advantages and disadvantages of each sensing scheme and adopts the proper scheme for our sensor system. A charge-sharing sensing scheme has a high sensitivity and a simple circuit structure for the restricted pixel area below a sensor plate. Table 1 shows the comparison of the capacitive sensing schemes.

This paper proposes an advanced sensor detection circuit for the capacitive fingerprint sensor signal processing. A detection circuit of charge sharing is proposed, which minimizes the influences of internal parasitic capacitances

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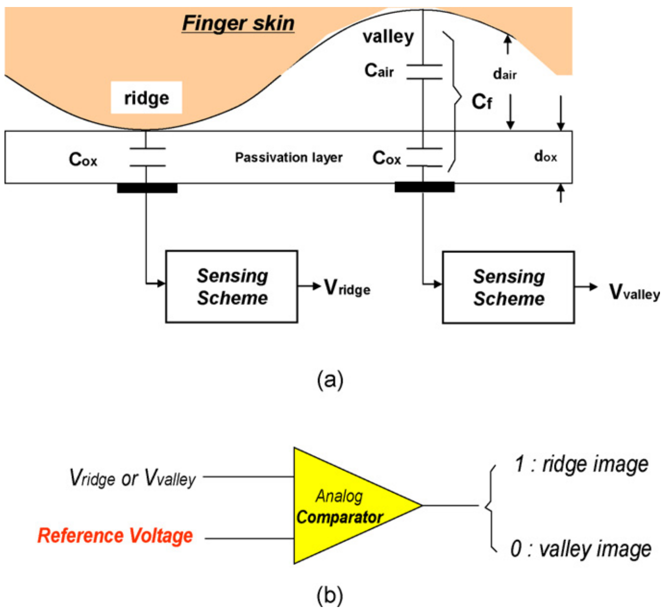

Fig. 1. Model of capacitive fingerprint sensing scheme: (a) capacitive fingerprint sensing scheme, (b) detection of a ridge and valley using comparator.

and enlarges the voltage difference between a ridge and valley.

Since the surface of a fingerprint sensor is exposed to capture a fingerprint image by finger touching, the condition of the sensor surface changes during long-term use. In other words, the sensor surface becomes dirty in practical use. Gradually, a parasitic capacitance is formed between the dirt and the sensor plate, and the sensed capacitance increases as a result. This means that the output signal from the fingerprint sensor depends on the sensor surface condition. Thus, the change of the surface condition degrades the captured fingerprint images. The degraded fingerprint images make accurate user authentication impossible. To achieve accurate authentication, the fingerprint sensor has to capture clear fingerprint images even though the sensor surface condition has changed. Conventional fingerprint sensors have no circuit technique that addresses this issue. To solve this problem, we propose a pixel-level automatic calibration circuit. This paper describes the pixel-level automatic calibration circuit

Table 1
Comparison of the capacitive sensing schemes

Sensor detection method	Advantage	Disadvantage
Charge sharing	Simple circuit	Influenced by a parasitic capacitance
	High image quality	
Charge transfer	Simple circuit	Sensitive on process variation
	Small leakage current	Weakness on noise
Feedback capacitive	High image quality	Charge injection Low image resolution
Sample and hold	Simple circuit	Use two dielectric materials by special sensor process Long image capture time

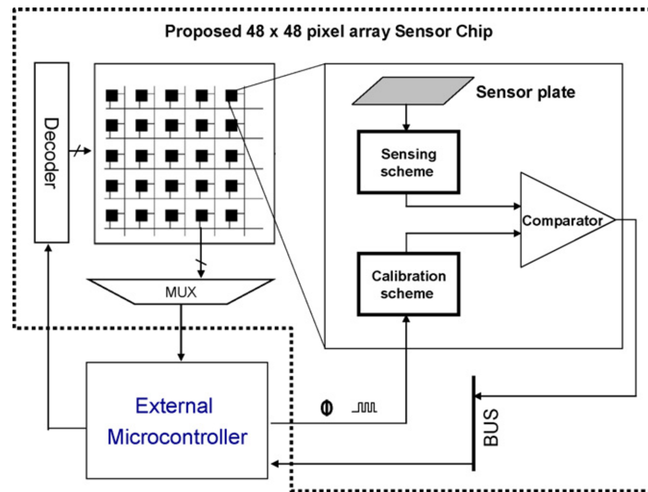

Fig. 2. Proposed fingerprint sensor block diagram.

scheme, which initializes the sensing characteristics and eliminates the influence of the sensor surface condition.

The new fingerprint sensor circuit is composed of the sensing scheme and calibration scheme as shown in Fig. 2. The test circuit is made with 0.35 μm CMOS processed 48 × 48 pixel array fingerprint sensor chip.

2. Fingerprint sensor circuit design

2.1. Sensing scheme

Fig. 3 shows a conventional charge-sharing sensing scheme and timing diagram. The capacitance of C_f is at its maximum value when a ridge has contact with the passivation layer. As the distance between the chip surface and the finger's skin increases, the capacitance becomes smaller.

In Fig. 3, "U-BUF" means a unit-gain buffer and "Comp" is a comparator. In the precharge mode, transistors M1, M3, and M4 are on, and M2 is off. The output of U-BUF and Vsa are precharged to VDD, and node C_{p2} is discharged to GND. In this mode, no charge is accumulated in C_{p2} and C_{p3} because the two electrodes have the same potential. In C_{p1} and C_f, the amount of charge stored is C_{p1}·VDD and C_f·VDD.

At the beginning of the unit-gain mode, the switches M1, M3 and M4 are turned off, and M2 is turned on. Then, the charges stored the precharge mode are redistributed between the nodes. The U-BUF tracks the voltage change of the node Vsa, which makes the potential difference between the two electrodes of C_{p3} zero. Usually, because C_{p1} and C_{p2} are the parasitic metal routing capacitances, they are much smaller than C_{p3}. Therefore, we need a circuit to remove the effect of C_{p3}. From this point of view, an application of U-BUF of Fig. 3 was an effective method [1]. But actually, the voltage is expected to be smaller than its value in silicon chip, because C_{p3} cannot be perfectly removed and the fabrication parameters can be changed. Therefore, ideally calculated voltage [1] is not sufficient to discriminate easily a ridge and valley because the reference voltage (V_{ref}) cannot be uniformed by voltage-down in each pixel of wide sensor area.