Sensors and Actuators A 147 (2008) 41–46

Contents lists available at ScienceDirect

Sensors and Actuators A: Physical

journal homepage: www.elsevier.com/locate/sna

First Vertical Hall Device in standard 0.35 μm CMOS technology

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ARTICLE INFO

Article history:
Received 23 October 2007
Received in revised form 9 January 2008
Accepted 3 March 2008
Available online 18 March 2008

Keywords:
Hall effect
Vertical Hall Device (VHD)
Standard CMOS technology

ABSTRACT

In order to lower the short-circuit effect due to the measurement contacts, Vertical Hall Devices (VHDs) are generally designed either in bulky N-type silicon or in the deep N-well of high-voltage CMOS technologies. In this last case, VHD can benefit from on chip circuitry for offset and 1/f noise reduction, but HVCMOS remains a costly technology. Using spinning-current, HVCMOS compatible VHDs with a resolution of 76 μT rms over a 1.6-kHz bandwidth have been demonstrated. The VHD presented here is designed in the shallow N-well of a low-cost 0.35 μm standard CMOS technology. Unlike conventional VHD, its measurement contacts are located outside the sensor active area. FEM simulations and experimental results show that the new geometry suppresses the short-circuit effect and strongly reduces the intrinsic offset and noise. Thus, without any noise and offset reduction method, this new small VHD (63 μm^2) reaches a resolution of 79 μT rms over a (5 Hz–1.6 kHz) bandwidth, and opens the way to the integration of 3D Hall sensors in low-cost standard CMOS technologies.

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1. Introduction

The Vertical Hall Device (VHD), which is sensitive to a magnetic field in the plane of the chip, was devised more than 20 years ago [1,2]. Such a device is also named parallel-field Hall microsensor [3–5]. Until now, it has been manufactured as a discrete component [6] because its biasing current has to flow in the depth of the device, preventing its integration since no current can be injected in the substrate of a CMOS circuit. Recently, a VHD designed with the deep N-well ($d_w = 7$ μm) of a high-voltage CMOS technology has been successfully demonstrated [7]. It has the advantage to be co-integratable with electronics to use spinning-current for offset, 1/f noise [8] as well as planar Hall effect [9] reduction. Combined with a conventional Horizontal Hall Device, it is at the origin of the first monolithic 3D Hall probe [10], which is now commercially available [11].

Nevertheless, such a VHD cannot be integrated in the thin N-well (depth $d_w = 2$ μm) of a standard CMOS technology because in that case a part of the biasing current flows through the sensing contacts instead of flowing through the low-doped N-well area beneath these contacts. The new vertical Hall effect sensor proposed in this paper addresses this issue. It is based on a structure similar to the one presented in [12,13], where the measuring contacts are located outside the sensor active area. Nevertheless, unlike the device presented in [12] which is realized as a discrete component, our sensor is integrated in a low-cost 0.35 μm CMOS process. Section 2 describes the working principle of our VHD and studies through F.E.M. simulations the limits in terms of sensitivity of Vertical Hall devices integrated in CMOS technologies. The advantage of using Hall contacts outside the sensor active area for device integration is also discussed. Section 3 compares the experimental results obtained with the conventional 5-contact VHD structure and with the new one proposed here. Finally, Section 4 concludes on this work and exposes the perspectives associated with these new results.

2. New vertical Hall effect device

2.1. The Hall effect

The working principle of a Hall effect device is depicted in Fig. 1.

When a magnetic field B_x is applied orthogonally to a semiconducting plate biased with a current I_p, a Hall voltage settles between the two lateral sides of the plate (Fig. 1) [6]. This voltage stems from the Hall electric field, which is given by:

$$\vec{E}_H = \frac{-r_H}{q \cdot n} \cdot \vec{j} \times \vec{B}$$

Such a plate is called a Horizontal Hall Device, since it is sensitive to the magnetic field B_x orthogonally oriented to the plane of the chip. r_H is the electron scattering factor (in silicon $r_H \approx 1.15$), q the elemental electric charge, n the doping level of the plate, $\vec{j}$ the current density, and $\vec{B}$ the magnetic field. By integrating the previous equation, the sensitivity of the Horizontal Hall Device is

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doi:10.1016/j.sna.2008.03.011

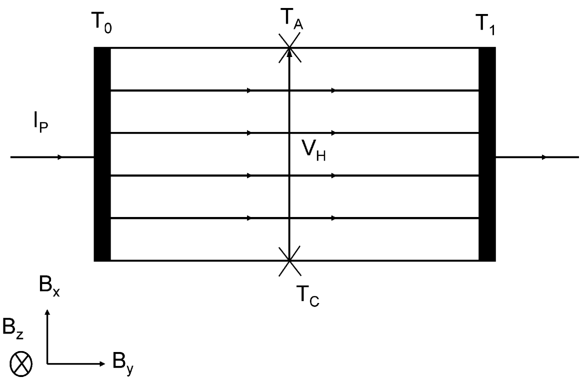

Fig. 1. Horizontal Hall plate.

obtained as [6]

$$S = \frac{V_H}{B} = \frac{G \cdot r_H}{n \cdot q \cdot t} \cdot I_P = S_I \cdot I_P$$

where t is the plate thickness and I_p the biasing current. G is the geometrical factor ($G < 1$) which models the reduction of V_H due to the part of the current which flows through the sensing contacts T_A and T_C as well as the short-circuit effect induced by the biasing contacts T_0 and T_1. S_I is the current-related sensitivity. We define $S_{Imax} = S_I$ when $G = 1$:

$$S_{Imax} = \frac{r_H}{n \cdot q \cdot t}$$

S_{Imax} only depends on the plate doping level n and on the thickness t. Thus, whatever the plate geometry is, the theoretical maximum sensitivity remains the same as long as $G = 1$. In particular, this is the case if biasing and sensing contacts are point like [6].

2.2. Conformal mapping and VHD structures

In the previous section, we mentioned that a horizontal Hall effect device is sensitive to the magnetic field orthogonally oriented to the plane of the chip. In addition, the current lines and the electric field lines form a constant angle $\theta_H = \mu_n B$, where μ_n is the carrier mobility and B the magnetic field component orthogonal to the current lines. Therefore, when performing a conformal mapping, which is a geometrical transformation that preserves the angles, we obtain an equivalent plate with a different geometry. Fig. 2 illustrates the bilinear transformation which transforms the unit circle in the complex t plane into the upper half plane in the complex z plane. As stated in the previous section, with point-like contacts, the unit circle is equivalent to a traditional Hall plate with a geometrical factor $G = 1$. Assume now that such a circle is placed vertically in the wafer. This structure is not practically feasible in a planar technology since contact T_1 would be then located in the depth of the substrate. On the contrary, the equivalent structure in the upper half plane of the complex z plane can be carried out in a CMOS planar process since all the contacts are located on the same side that is the top side of the wafer. Practically, the Vertical Hall Device is implemented in the N-well of the CMOS technology and exhibits finite dimensions. In particular, the VHD depth is limited to roughly 2 μm in a low-cost standard 0.35 μm CMOS process. As a matter of fact, each structure is sensitive to the magnetic field orthogonally oriented to the current lines. Current lines flow from T_0 to T_1 in the t plane and from Z_0 to $Z_{1,1'}$ in the z plane. Note that after transformation, Z_1 and $Z_{1'}$ become infinitely long.

In the t plane, the Hall voltage is measured between T_A and T_C, $V_H = V_{T_A - T_B} + V_{T_B - T_C}$ where T_B is the center of the circle (Fig. 2). Due to the central symmetry, the V_{T_B} potential does not change whatever the value of the magnetic field applied to the circular device is. On the contrary, for its counterpart in the non-infinitely deep z plane, this is not the case (see Section 2.3), and to measure the same sum of voltages in the z plane, we need an access to the rear side of the N-well, that means to points Z_B and $Z_{B'}$ (which are not located at the infinite in the N-well deepness as they should be theoretically). In that configuration, we could have the same Hall voltage as in the t plane $V_H = V_{Z_A - Z_B} + V_{Z_{B'} - Z_C} = V_{T_A - T_C}$. Of course, that is not possible in planar technology since we have no access to Z_B and $Z_{B'}$. Hence, measuring the Hall voltage in the z plane does not permit to obtain 100% of the theoretical sensitivity S_{Imax}. It is important to note that even if the VHD is deep enough for the Hall voltage to vanish at the rear side, a Hall voltage will then settle at the lateral sides, whatever the distance between these lateral sides is. In other words, using planar technologies with all the contacts on the same side, the sensitivity measured between two sensing contacts of any VHD will be only a fraction of S_{Imax}, whatever the relative location of the sensing and biasing contacts is, these contacts being point-like or not.

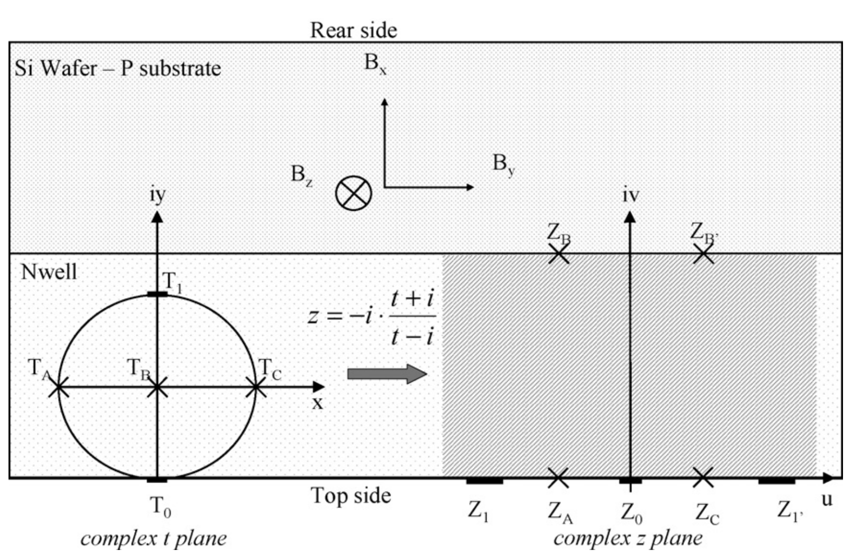

Fig. 2. Bilinear transformation. The top side of the wafer corresponds to the bottom side of the figure.

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