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Solid-State Electronics 49 (2005) 1702–1707
SOLID-STATE ELECTRONICS
www.elsevier.com/locate/sse

A spice-like reliability model for deep-submicron CMOS technology

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Received 25 May 2005; received in revised form 2 September 2005; accepted 2 September 2005

The review of this paper was arranged by Prof. A. Zaslavsky

Abstract

Continuing down scaling in CMOS technology has resulted in an increasing and urgent need for a Spice-like reliability model that is capable of predicting the long-term degradation of MOS devices and ICs. In this paper, we develop such a model based on the industry standard BSIM3 model and empirical degradation expressions for the threshold voltage and mobility of MOSFETs. The model is implemented in Cadence Spectre via Verilog-A, and good agreements between the measured and simulated results have been obtained for devices fabricated from the 0.18-μm CMOS technology.

Keywords: MOS devices; Reliability; Hot-carrier stress

1. Introduction

Due to the continuing down scaling, the hot-carrier (HC) effect becomes more significant in modern deep-submicron MOS devices [1]. The great majority of the MOS reliability studies reported in the literature has focused on the physical mechanisms associated with the gate leakage current and substrate current caused by the hot-carrier effect [2–10]. Empirical models for MOS degradation due to the hot-carrier effect have also been developed [11,12]. However, a Spice-like MOS model which is capable of predicting the degradation of MOS devices and circuits as a function of the stress condition has largely been overlooked and not well established in the semiconductor device community.

In this paper, we seek to develop an MOS reliability model for circuit simulation. The model will be derived based on the industry standard BSIM3 framework [13] with the relevant degradation physics incorporated. The model will then be implemented into Cadence Spectre via Verilog-A language. Measured data will also be included in support of the model development.

2. Model development

A widely used methodology for MOS reliability simulation combines the Berkeley Reliability Tools (BERT) and Cadence Spectre. The BERT model assumes that all Spice model parameters degradation follows the equations:

$$\Delta D = f(AGE) \tag{1}$$

$$AGE = \int_0^{\tau} \frac{I_{DS}}{W \cdot H_S} \left[\frac{I_{SUB}}{I_{DS}}\right]^{m_S} \mathrm{d}t \tag{2}$$

where ΔD is the amount of degradation of a MOSFET character D (i.e., transconductance or threshold voltage), W is the device width, H_S and m_S are fitting parameters determined experimentally from a given technology, I_{SUB} is the substrate current, I_{DS} the drain current, and τ is the stress time. It has been suggested, however, that modern MOSFETs with a very thin gate oxide exhibit better reliability than that predicted by (1) and (2) over a wide range of bias conditions and gate lengths [9]. An improved MOS reliability model will be developed below.

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doi:10.1016/j.sse.2005.09.003

Table 1
Effect of changing BSIM DC parameters on MOS DC and RF performance

BSIM parameters	BSIM parameter 10% change				BSIM parameter 30% change			
	DC performance		AC performance		DC performance		AC performance	
	0.1 V (%)	1.8 V (%)	1 G (%)	3 G (%)	0.1 V (%)	1.8 V (%)	1 G (%)	3 G (%)
VTH0	4.08	5.64	0.65	0.64	12.35	16.73	2.52	2.41
U0	4.83	2.42	1.36	1.23	15.46	8.48	5.14	4.62
UA	2.00	0.98	0.69	0.67	5.66	2.88	2.09	2.00
UB	3.16	1.55	1.43	1.40	8.72	4.51	3.87	3.74
ETAB	<0.1	<0.1	<0.1	<0.1	<0.1	0.19	<0.1	<0.1
PDIBLC2	<0.1	<0.1	1.42	1.12	<0.1	<0.1	4.10	5.33
JSW	<0.1	<0.1	<0.1	<0.1	<0.1	<0.1	<0.1	<0.1
JS	<0.1	<0.1	<0.1	<0.1	<0.1	<0.1	<0.1	<0.1
PB	<0.1	<0.1	<0.1	0.17	<0.1	<0.1	0.19	0.47

The devices under study are n-channel MOSFETs fabricated with the 0.18-μm CMOS technology. The channel width is 10 μm, and device make-up includes P-well, N-well, threshold-adjust implant, and retrograde doping profiles.

Industry standard BSIM3v3 model developed by UC Berkeley is used as the backbone of our model development. A sensitivity analysis is first carried out to determine which BSIM parameters influence most significantly the MOS characteristics when the values of these parameters are changed. Once these parameters are known, stress-dependent expressions are then derived empirically using measured data. Finally, these parameters are incorporated into Cadence Spectre for MOS reliability simulation.

For the sensitivity analysis, main dc and ac BSIM parameters are varied by 10% and 30%, and their effects on the dc (drain current I_{DS} at gate voltage $V_G = 1.6$ V and drain voltage $V_D = 0.1$ V and 1.8 V) and ac (S21 magnitude at $V_G = 0.9$ V and $V_D = 1.8$ V) performances are simulated. Tables 1 and 2 summarize the sensitivity analysis of the dc and ac parameters, respectively, and the results suggest that changing any of the ac parameter alters minimally the MOS RF behavior and that only the threshold voltage V_{TH} and effective mobility μ_{eff} influence significantly the MOSFET dc and RF performances. Thus, stress-dependent expressions will be derived below for these two parameters.

Table 2
Effect of changing BSIM AC parameters on MOS RF performance

BSIM parameters	BSIM parameter 10% change AC performance		BSIM parameter 30% change AC performance	
	1 G (%)	3 G (%)	1 G (%)	3 G (%)
Cit	<0.1	<0.1	<0.1	<0.1
CGSO	<0.1	<0.1	<0.1	<0.1
CGDO	<0.1	<0.1	<0.1	<0.1
CGBO	<0.1	<0.1	<0.1	<0.1
MJ	<0.1	<0.1	<0.1	<0.1
PBSW	<0.1	<0.1	<0.1	<0.1
MJSW	<0.1	<0.1	<0.1	<0.1
PBSWG	<0.1	<0.1	<0.1	<0.1
MJSWG	<0.1	<0.1	<0.1	<0.1

The threshold voltage in BSIM3 is expressed as

$$V_{TH} = \mathrm{VTH0} + \delta_{NP}(\Delta V_{T,body\_effect} - \Delta V_{T,charge\_sharing} - \Delta V_{T,DIBL} + \Delta V_{T,reverse\_short\_channel} + \Delta V_{T,narrow\_width} + \Delta V_{T,small\_size}) \quad (3)$$

It can also be extracted experimentally from

$$V_{TH} = V_{G\_max} - \frac{I_{DS\_max}}{G_{m\_max}} - \frac{V_{DS}}{2} \quad (4)$$

Here V_{G_max} and I_{DS_max} are V_G and I_{DS} at maximum transconductance G_m. Fig. 1 shows the measured drain current vs. gate voltage characteristics, which yields $V_{TH} = 0.517$ V using (4). On the other hand, $V_{TH} = 0.510$ V is calculated from the expression in (3). This demonstrates the accuracy of the threshold voltage model in BSIM3. Note that the threshold voltage mentioned above is the threshold voltage of a fresh MOSFET.

For a fixed stress condition, the degradation of V_{TH} obeys the power law

$$\frac{dV_{TH}}{V_{TH}(0)} = A \cdot t^n \quad (5)$$

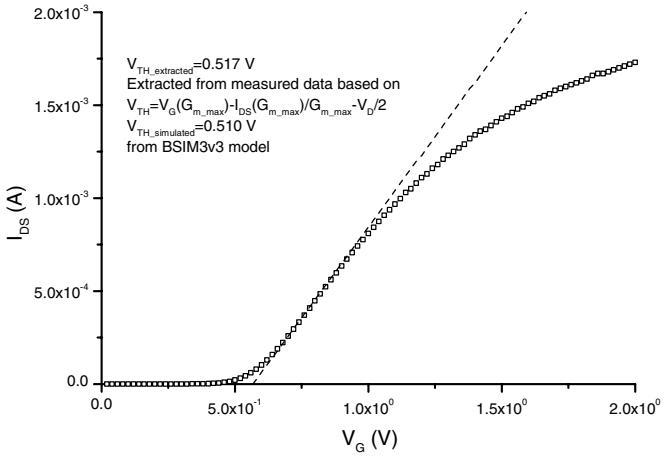

Fig. 1. Current–voltage characteristics showing the extraction of threshold voltage. The drain voltage used is 0.1 V.