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High-voltage solutions in CMOS technology

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Abstract

This paper presents trends on CMOS high-voltage techniques for power integrated circuits (PICs). Several fully CMOS compatible drain engineering techniques will be presented. Experimental devices were fabricated in standard CMOS processes from three different lithography generations (2, 0.7 and 0.5 μm) without resorting to any extra processing steps. MOS devices layout specificity towards performance improvement, namely breakdown, parasitic effects and degradation, will be emphasized.

A recently developed technique used to enlarge high-voltage devices safe-operating area and reduce leakage current will also be presented due to the very promising experimental results.

Comparison with more sophisticated and expensive technologies still reveals CMOS as a highly accessible and versatile technology for future PICs.

Keywords: High-voltage; Power integrated circuits; CMOS compatible

1. Introduction

Power integrated circuits (PICs), tailored for power electronics applications (drivers, actuators, regulators, etc.), that require voltages higher than standard 5-volt digital CMOS processes, are usually fabricated either resorting to expensive solutions, (e.g. BCD), or even to dedicated smart power technologies [1]. State-of-the-art semiconductor devices, like MOSFETs, IGBTs or TrenchFETs, are used, in all cases, as switching devices, with extremely low voltage drops at on-state, low leakage current at off-state and ultra-fast switching times, features that are crucial to attain low power losses and thus increased circuit efficiency.

MOSFETs are usually the preferred switching devices to be included in PICs for applications below 100 V. MOSFETs, as PICs main power switching cell, either in a lateral (LDMOS) or in a vertical structure (VDMOS), present two important advantages: (1) extremely low switching times; (2) less complex drive, control and protection circuits, laid into a few mm^2 area in the same monolithic circuit.

In the last decade, a reasonable effort concerning the development of PICs led some previously proposed solutions to miniaturization in order to obtain improved overall power electronics systems reliability. However, the optimistic expectation of 'everything inside a chip' did not succeed in the power microelectronics market, especially due to the fact that technological processes are still very expensive and independent research teams have restricted access to them. Consequently, several works have been reported, which consider the possibility of using CMOS, BiCMOS, BCD or even smart power dedicated technologies to develop PICs [2–11]. Some of these works refer CMOS or BiCMOS process flow modifications, either by including additional masks and/or additional doped regions [4,7]. However, only a few of these solutions are fully compatible with the available cost effective technologies [3,5,6,11].

In order to contribute to overpass some of these restrictions, this work will discuss trade-offs and viability of several solutions towards the integration of HV MOSFETs in standard CMOS processes, without modification of processing steps. The main target is the development of a HV MOSFETs library in standard CMOS technology, for foundries and designers use, aimed at implementing the functionalities required by PICs power control. In this way, interesting design solutions will become available for the development of very low cost PICs, what will strongly increase expectations in this area.

2. Standard CMOS technology

Available CMOS standard processes were designed to

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provide high performance NMOS and PMOS devices for digital and/or low power analog applications. The use of CMOS standard technologies for HV applications, without changes in process flow, involves a deep knowledge of technology parameters and mask generation, in order to permit the design of devices in compliance with reliability and performance specifications.

Usually, CMOS technology is characterized by three main parameters: the minimum lithographic length, the well doping type and the number of available polysilicon and metal interconnection layers. CMOS processes can be n-well, p-well or twin-tub. All experimental HV devices presented in this contribution are NMOS transistors. However, the fabrication of PMOS devices is also possible, with both n-well and p-well processes. On the other hand, the fabrication of PMOS devices in a twin-tub process could become a difficult or even impossible task, depending on foundry policy and on the versatility of mask generation and preparation.

Experimental data discussed in this work were obtained using prototypes fabricated in three CMOS processes, originally targeted at digital applications: a 2 and a 0.7 μm CMOS process, both with n-well on p-substrate, and a 0.5 μm twin-well process.

2.1. CMOS processes and structures

Most CMOS standard processes obey to similar process flows to obtain the complementary NMOS and PMOS devices. For a typical n-well process, the process flow can be summarized as follows:

- well implantation, in order to provide a deep substrate for the PMOS transistors;
- active area definition, where drain and source implants n + and p + will subsequently be laid;
- field-oxide (FOX) growth, to provide isolation between complementary transistors;
- p-type transistor threshold voltage adjustment implantation, high quality Gate oxide growth and polysilicon deposition;
- source and drain implantation and subsequent metal layers deposition, with CVD SiO_2 dielectric isolation between them.

A typical cross-section obtained through this process is shown in Fig. 1.

The deep n-well doping profile is one of the most important characteristics involved in the design of the HV modified structures proposed in this paper. N-well surface concentration and depth depend on process scale and substrate concentration. The inclusion of this layer in the drain of the proposed HV structures will be responsible for the device blocking voltage increase, due to its lightly doped concentration in comparison with the standard MOS n+ implants. It will also be shown that the p-type field

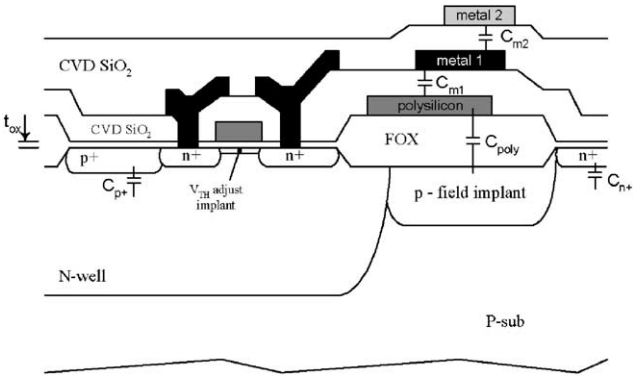

Fig. 1. Cross-section for an N-well CMOS typical process.

implant, used as a 'channel stop' in digital applications, will play an important role in the improved performance of the proposed CMOS compatible HV structures.

Since digital CMOS are tailored typically for 5 V or less, the possibility of an increase in voltages applied to in chip devices must be carefully studied, in order to maintain the expected reliability and device robustness. On the other hand, for high power demanding applications, gate voltages should be increased above the typical 5 V, what could become a major risk when hot carrier degradation, and subsequently reliability, comes in order. Thus, HV solutions in CMOS must always bring into discussion performance restrictions due to overdrive gate voltages. Preliminary evaluation of the maximum allowable voltage that can be applied to a digital CMOS Gate oxide for a long-term reliability (10-year lifetime period, at 125 °C) can be estimated from time to breakdown, t_{BD} [12].

Independent PICs designers that use these CMOS technologies will face foundry IC process confidentiality. In fact, only design rules and a few aspects of electrical rules are available. Details of process parameters, such as n-well, field and threshold voltage adjustment implants concentrations and energies, drive-in time and temperature, etc., are part of restricted documentation, not accessible for design purposes outside the foundry. Designing semiconductor devices without approximate values for cross-section dimensions and process parameters (i.e. substrate resistivity, diffusions and implants doping profiles, distance between layers above silicon and corresponding thickness) requires a high number of test structures per prototype and long prototyping cycles, together with a significant increase of development phase cost. Thus, it is crucial to find, at least, an approximation of the above mentioned characteristics, in order to reduce cost and time in the development of new HV solutions for CMOS technology, either resorting to two-dimensional simulators or to analytical models.

2.2. Parameter extraction for 2D simulation of HV structures

Two-dimensional (2D) device simulation is a powerful tool that permits to spare time in the development cycle, especially