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Transistor optimisation for a low cost, high performance 0.13 μm CMOS technology

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Abstract

This paper discusses the optimisation of a high performance, low cost 0.13 μm CMOS technology with a view on its further scaling to the 100 nm technology node. The focus is mainly on gate oxide (thickness and nitridation method), deep junction implants and annealing. It is shown that in order to take the full benefit of gate oxide thinning, low energy boron implants and spike rapid thermal anneal are mandatory for pMOS devices. The same route gives also promising results for nMOS transistors when gate predoping is used to reduce gate depletion.

Keywords: CMOS processing; Nitrided oxide; Boron ion implantation; BF_2 ion implantation; Spike rapid thermal anneal

1. Introduction

Gate and source/drain engineering are two key aspects of deep-submicron device optimisation. It has now been widely agreed that the 100 nm CMOS technology node will feature surface channel devices with polysilicon gate [1]. As a result, gate engineering consists in that case in minimising both n-gate depletion and boron penetration, while preserving interface quality. Keeping in mind the constraints due to thermal budget, this can be done by combining as-deposited polysilicon with nitrided gate oxide. Two routes were looked at to provide nitrogen-rich gate oxide [2]. The first one consists in first growing pure silicon dioxide and then incorporating nitrogen via an anneal in NO ambient. In this way, the nitrogen is mostly present at the channel-to-oxide interface where it severely impacts on hole mobility [2] and current noise [3]. The second approach is about the opposite: first, nitrogen-rich oxide is grown in NO ambient and it then reoxidised in normal conditions. With this method, the nitrogen peak is closer to the polysilicon-to-oxide interface and the channel interface properties are nearer to those of pure oxide [2]. Beside gate optimisation, source/drain engineering is needed to control short channel effects while minimising series resistance.

For these reasons, we present the optimisation of 0.13 μm transistors with a view to further scaling to the 100 nm node, and with special attention paid to gate oxide (thinning, nitridation recipe), deep junction implant and thermal budget.

2. Device fabrication

The reference process flow starts with shallow trench isolation and dual well formation with retrograde profiles, targeting at ±0.3 V long channel threshold voltage (V_{th}). The gate stack consists of 2.0 nm NO-annealed oxide covered with 150 nm of polysilicon. After gate patterning using 248 nm DUV lithography with alternating phase-shift masks, optimised shallow n- and p-extensions are formed with respectively. As (5 keV) and

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BF_2 (6 keV), together with corresponding BF_2 (65 keV) and As (120 keV) halo implants [4]. Following, 80 nm-wide nitride spacers are formed and highly doped drain (HDD) implant is carried out, using As at 50 keV for nMOS and B at 6 keV for pMOS. After soak rapid thermal anneal (RTA) at 1050 °C and advanced Co-salicidation with a Ti cap [5], the processing is conventional.

Process variants were introduced to investigate the influence of gate oxide thickness/recipe (2.0 nm reoxidised NO oxide, 2.5 nm NO-annealed oxide), shallower HDD implants, and junction RTA (spike RTA vs. the reference soak anneal). It is worth mentioning that different V_{th}-adjust doses were used for the two oxide thicknesses.

3. Impact of gate oxide thickness and recipe

The V_{th} roll-off of nMOS devices with the various nitrided gate oxides is presented in Fig. 1 (top). Comparing the two 2.0 nm recipes, it is first noticeable that both nitridation schemes (pre or postnitration) give the same amount of fixed charges and the same boron diffusivity in the channel, in contrast to what was already reported for thicker layers [2]. When examining the I_{on}–I_{off} characteristics in the bottom part of Fig. 1, the 20% gate capacitance increase (from oxide thinning) turns directly into 20% drive improvement at constant leakage, leading to a working point of 890 μA/μm with 2 nA/μm leakage at 1.5 V bias for 0.13 μm gate length.

Likewise, pMOS V_{th} roll-off in Fig. 2 (top) points to a better boron-penetration blocking by using reoxidised oxide, since the latter improves long channel V_{th} by about 30 mV with respect to NO-annealed 2.0 nm oxide. This could be expected from the position of the nitrogen peak within the oxide: in contrast to NO-annealed oxides, reoxidised layers have this peak located closer to the polysilicon interface, with a better boron blocking effect and improved hole effective mobility [2]. When examining transistor performance in Fig. 2 (bottom), it is striking that the 20% oxide thinning only results in 10% drive gain at constant bias, with a best performance of 390 μA/μm at 2 nA/μm leakage at 1.5 V bias.

This limited performance improvement can be explained by comparing the top and bottom parts of Fig. 3, showing normalised drain-induced barrier lowering effect (DIBL) vs. gate length for n and pMOS, respectively. Although the increase in gate capacitance results in reduced DIBL for nMOS, it does not seem to improve gate-to-channel coupling in short channel pMOS. This is most likely because the deep 6 keV boron HDD overrules p-extension and determines short channel

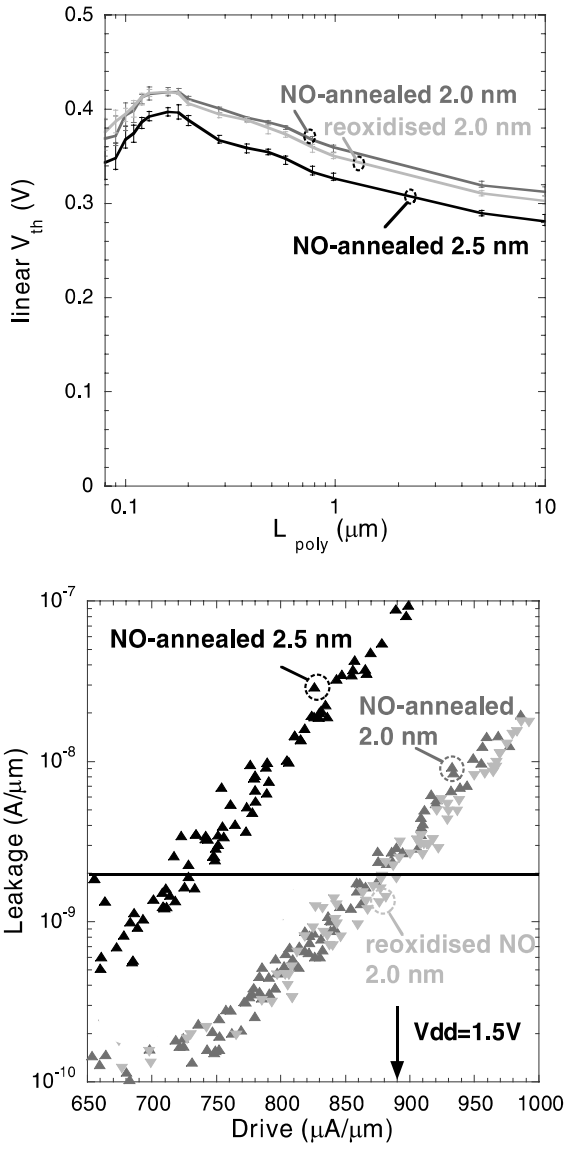

Fig. 1. Linear V_{th} (top) and I_{on}–I_{off} (bottom) for nMOSFETs featuring various gate oxides.

effects. To verify this hypothesis, shallower p-HDD was looked at.

4. Shallow HDD and spike RTA

To create shallower p-type source/drain regions, BF_2 was implanted at 14 keV (equivalent to boron at 3 keV) with the reference dose. As fluorine enhances boron penetration with soak anneals [6], the BF_2 implant was used in conjunction with much reduced thermal budget