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Ultra-thin silicon nitride by hot wire chemical vapor deposition (HWCVD) for deep sub-micron CMOS technologies

Parag C. Waghmare[a,*], Samadhan B. Patil[a], Alka Kumbhar[a], R.O. Dusane[a], V. Ramgopal Rao[b]

[a]*Department of Metallurgical Engineering and Materials Science, Indian Institute of Technology, Bombay, Powai, Mumbai 400 076, India*

[b]*Department of Electrical Engineering, Indian Institute of Technology, Bombay, Powai, Mumbai 400 076, India*

Abstract

Silicon nitride is considered a promising candidate to replace thermal oxide dielectrics, as the latter is reaching its scaling limits due to the excessive increase in the gate tunneling leakage current. The novel hot wire chemical vapor deposition (HWCVD) technique shows promise for gate quality silicon nitride film yields at 250 °C while maintaining their primary advantage of a higher dielectric constant of 7.1. In this paper we report the results of our efforts towards developing ultra-thin HWCVD silicon nitride as an advanced gate dielectric for the replacement of thermal gate oxides in future generations of ultra large scale integration (ULSI) devices.

Keywords: Low-temperature silicon nitride (Si_3N_4); High-*K* dielectric; HWCVD

1. Introduction

The semiconductor industry has maintained its aggressive pace of growth by improving performance and reducing the cost per function of integrated circuits. Shrinking of device dimensions is the primary cause for this improvement as it can offer both an increase in speed as well as density of devices on the chip [1]. Successful shrinking of the device is achieved by reducing both horizontal and vertical dimensions according to the scaling rules. Thus, as the channel length of the device is reduced, the thickness of the gate dielectric must also be scaled in today's metal oxide semiconductor (MOS) devices to maintain good short channel performance.

*Corresponding author. Tel.: +91-22-572-3655; fax: +91-22-572-3480.
E-mail address: parag@met.iitb.ac.in (P.C. Waghmare).

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One major problem with the scaling of the oxide thickness (1.5–2.0 nm) is the excessive increase in the leakage current due to direct tunneling [2]. Penetration of boron through the gate oxide into the silicon substrate in the fabrication of surface channel P-MOSFET is also a limiting factor. Growing such a thin film uniformly across wafers of 200–300 mm diameter is a formidable task. Thus, if the scaling trend is to be sustained, an alternative gate dielectric must be found that can be used as a viable replacement for silicon oxide [3]. One way to extend the scaling of MOS devices is to use another material with a dielectric constant and physical thickness higher than that of silicon oxide to maintain the same gate insulator capacitance value according to the scaling rules. Various high-K dielectrics have been under investigation by researchers and it is well known that the material that can replace silicon oxide has to meet several stringent requirements concerning bulk and interface quality and should be compatible with conventional CMOS technology.

Silicon nitride, among other high-K dielectrics, is at the forefront of research, as it has a dielectric constant twice that of silicon oxide. It is also very resistant to the penetration of impurities such as boron and sodium and acts as a good passivating layer for moisture-related effects [3].

In this paper we report MOS capacitors made with ultra-thin [< 4 nm EOT (effective oxide thickness)] silicon nitride by HWCVD as the gate dielectric. Detailed electrical characterization has been carried out and reliability issues such as high breakdown strength and very little trap generation by these devices have also been addressed.

2. Fabrication

a-SiN:H films were deposited by HWCVD using Matheson grade SiH_4 and NH_3 on crystalline silicon (P-type, $\langle 100 \rangle$ orientation, 0.8–1.2 Ω cm resistivity) and corning 7059 glass substrates. The silicon wafers were chemically cleaned using the standard RCA cleaning procedure. Process parameters for a-SiN:H depositions are shown in Table 1.

The film thickness was measured using a dektak II surface profilometer by creating a step by masking a small area of the substrate during deposition. The thickness was verified by comparison with the thickness obtained from C–V measurements carried out on the MNS capacitor structure. IR absorption spectra of the films deposited on silicon substrates were recorded on a nicolet FTIR spectrometer in the range 400–4000 cm^{-1}. Al gate silicon nitride MNS capacitors were fabricated for electrical characterization. Post-deposition annealing was carried out for 20 min at 850 °C in a nitrogen atmosphere. Front and back metallization was performed using an Edward's E-beam evaporation system. A metal mask of area $0.785E-2$ cm^2 was used for defining the gate area. Post-metallization annealing (PMA) was performed for 20 min at 420 °C in a nitrogen atmosphere.

Table 1
Process parameters for a-SiN:H deposition

Gases used	SiH_4, NH_3
NH_3/SiH_4 flow rate ratio	10–50
Substrate temperature (T_s)	250 °C
Filament temperature (T_f)	1800 °C
Total gas pressure	30–250 mTorr
Deposition time	40 s
Distance between filament and substrate	5 cm