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Low voltage ride-through capability improvement of DFIG-based wind turbines under unbalanced voltage dips

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ABSTRACT

This paper proposes a competent and effective scheme to enhance the ride-through capability of DFIG-based wind turbines under unbalanced voltage dip conditions. The proposed method is realized through joint use of the rotor-side converter control and a three-phase stator damping resistor (SDR) placed in series with the stator windings. By means of an asymmetrical SDR idea, during the unbalanced voltage dip the SDR resistors are activated only in phase(s) experiencing low voltage. Then, the rotor current is controlled such that no unbalance voltage appears on the stator voltage. The proposed ride-through approach limits the peak values of the rotor inrush current, electromagnetic torque and DFIG transient response at the times of occurrence and clearing the fault. It also suppresses fluctuation of the electromagnetic torque and DFIG transient response appeared during unbalanced voltage dips due to negative sequence component.

1. Introduction

Variable-speed wind turbines (WTs) can offer increased efficiency in capturing the energy from wind over a wider range of wind speeds, along with better power quality [1]. Currently the preferred configuration for variable speed wind turbine is doubly fed induction generator [2]. Wind generation based on DFIG system results in lower converter cost and lower power losses compared to a system based on a fully fed synchronous generator with full-rated converter [3].

Doubly fed induction generator consists of a wound rotor induction generator with back-to-back voltage source converters linking the rotor to the grid. The rotor-side converter (RSC) is used to control the generator real and reactive power, while the grid-side converter (GSC) is used to control the dc-link voltage and reactive power exchanged with the grid [4]. Fig. 1 shows the schematic diagram of a DFIG-based WT connected to the grid through parallel lines and transformers.

The most common requirements of different countries for wind farm connection to grid include low voltage ride-through capability, frequency regulation ability and reactive power support [5]. DFIGs are very sensitive to the grid voltage dips. This is because the voltage dips induce large voltages in the rotor windings, resulting in high rotor current [4]. This high current can damage the RSC, and may cause large increase in the dc-link voltage. In spite of this problem, new standards and grid codes require that WTs remain connected to the grid during the voltage dip to realize the ride-through capability [6]. Also, it is necessary that wind turbine generators fulfill reactive power requirement during faults and post-faults periods, when the generator is allowed to remain connected to the grid [7].

The low voltage ride-through (LVRT) issue in DFIGs has been addressed by several countermeasures in the literature. The conventional method of using a crowbar [8–10], machine demagnetization through modified RSC control [11–13], compensation of rotor back-emf voltages [14], hardware modification and series voltage compensation by the voltage source converters (VSCs) [15,16] are the ride-through approaches proposed in the literature. However, they mainly deal with the DFIG LVRT behavior under balanced voltage dips.

To the contrary, unbalanced voltage dips are more common in power systems. In comparison to balanced voltage dips, for the unbalanced voltage dips, severity of transients at the times of beginning and clearing the fault may be lower. However, undamped oscillations appear in the DFIG response remaining throughout the unbalanced fault. These oscillations can be harmful for the WT drive train. Therefore, it is necessary that the LVRT

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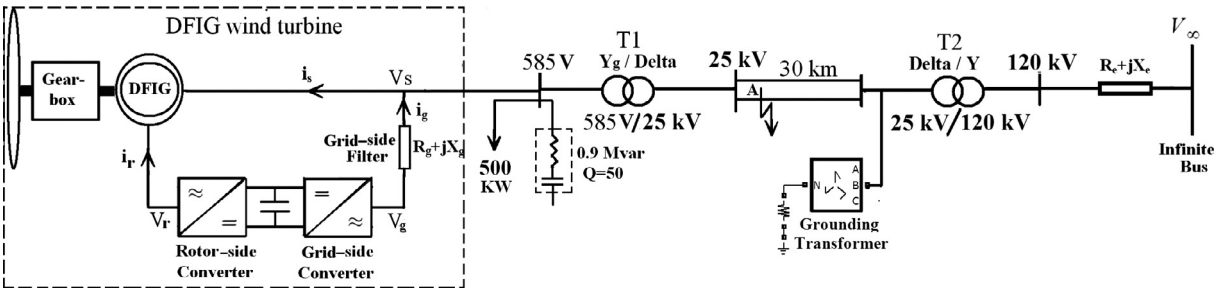

Fig. 1. Schematic diagram of the study system.

capability of the DFIG under unbalanced voltage dips be also taken into consideration.

Normally, it is more difficult to realize LVRT for DFIG under unbalanced voltage dips than in balanced voltage dips. In [17–19], the LVRT requirement of DFIG under unbalanced voltage dips has been addressed. These approaches are realized either by modifying the DFIG converter controls [17,18], or by using additional power electronic hardware [19]. The LVRT methods fulfilled through DFIG control modification can provide adequate response when the voltage dip and negative sequence content of the stator voltage are moderate. Hardware modification and using a series-connected VSC, as an alternative approach to meet the LVRT requirement, is technically feasible, but requires additional converters and other equipment which are costly.

In [20] the authors proposed an efficient method to improve the LVRT capability of the DFIG under balanced voltage dips. This method is mainly realized by using a passive resistive hardware called stator damping resistor (SDR), located in series with the stator windings. SDR consists of three resistors in parallel with three bypassing bidirectional static switches, as shown in Fig. 2. In normal conditions, the bidirectional static switches remain closed, and the stator current will not flow through the SDR resistors.

When a voltage drop is detected in the grid, the switches are turned off and the stator current flows through the series resistors. As discussed in [20], the SDR method can successfully enhance the DFIG voltage dip behavior without deactivating the generator converter. It reduces the peak rotor fault current and minimizes transient oscillations of electrical torque, rotor instantaneous power and DFIG transient response. In contrast to the other approaches, such as crowbar and series voltage compensation by power electronic converters, SDR is simpler and more cost effective with efficient performance.

The power losses of the bidirectional switches used in the SDR include conduction loss, during normal conditions, and switching loss at the events of the series resistors activation and deactivation. Since the system faults are infrequent and short, the latter component is insignificant, and dominant losses are of conduction type. The IGBT switches to be used for this purpose can be optimized either for lower conduction loss and or for lower switching loss. Thus, it is possible to adjust the optimization of the silicon design to maximize system benefits [21]. Therefore, appropriate selection of the semiconductor switches will limit the SDR losses and preserve high efficiency of the system.

This paper proposes a method to improve the LVRT capability of the DFIG under unbalanced voltage dips. This method is realized through joint use of RSC control and an asymmetrical SDR concept. The asymmetrical SDR is based on the SDR hardware in which the SDR resistors, under unbalanced voltage dip, are activated only in phase(s) experiencing low voltage. Then, the rotor current is controlled such that in spite of presence of negative sequence component in the grid voltage, no unbalance voltage appears on the stator voltage. Consequently, undamped negative sequence oscillations of the DFIG transient response is removed, and the DFIG LVRT capability is enhanced under unbalanced voltage dip. Also, reactive power requirement of the grid during the fault, according to grid codes, is addressed through GSC control. Hence, the main contribution of the proposed LVRT approach is that it can significantly balance the three-phase stator voltage, and consequently reduces the negative sequence components of the stator voltage to a negligible value during unbalanced voltage dips. This in turn leads to approximately balanced stator and rotor current/voltage with low negative sequence oscillations in electromagnetic torque and generator electrical variables.

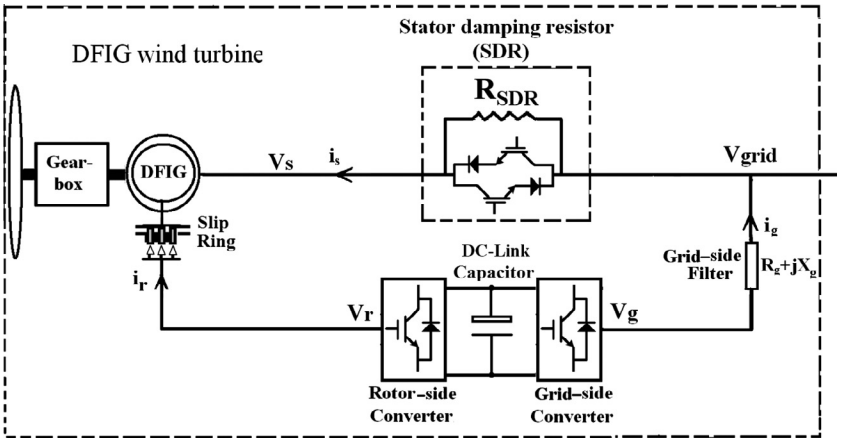

Fig. 2. Schematic diagram of SDR.