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FPGA-based reconfigurable control for switch fault tolerant operation of WECS with DFIG without redundancy

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A B S T R A C T

This paper deals with reconfigurable back-to-back converter topology and control orders in Wind Energy Conversion Systems (WECS). A typical WECS with Doubly Fed Induction Generator (DFIG) in balanced conditions is concerned. Based on the classical topology, a fault tolerant converter without any redundancy has been studied. The presented fault tolerant topology allows a "five-leg" structure with converters reconfiguration after switch failure detection. Furthermore, the control strategy for classical topology can no longer be applied after fault occurrence. Thus, a "five-leg" control strategy has also been proposed. The validation of the reconfigurable digital controller for the studied WECS with DFIG topology has been performed using a Hardware-in-the-Loop (HIL) reconfigurable platform including a Field Programmable Gate Array (FPGA) chip. HIL simulation results in both healthy and fault conditions have been presented to show simultaneously the viability of the studied converters topology and the reconfigurable control.

1. Introduction

At the end of 2011, the installed wind power in Europe was around 97 GW [1]. According to European wind energy association, wind turbines could provide 49% of EU electricity in 2050 [2]. Global market of wind energy is clearly expanding steadily, and consequently the technologic competition in this area has been accelerated. The demand for continuously available power electronics systems is increasing. Most loads that are fed by power systems require non-stop and fault tolerant operation. Wind Energy Conversion Systems (WECS) are typical application cases where the efficient production is directly linked to economic benefits [3,4]. More particularly, WECS are sensitive to power switch failure. A sudden failure in one of the power switches decreases system performance and can lead to disconnection of the power system. More, if the fault cannot be quickly detected and compensated, it can lead to hardware failure. In Ref. [5], a power switch failure detection for three-leg fault tolerant converter topology has been developed. This approach minimizes the time interval between the fault occurrence and its diagnosis. The possibility to detect a faulty switch in less than 10 μs by using a diagnosis simultaneously based on a "time criterion" and a "voltage criterion" has been demonstrated. In order to perform such a short detection time, a Field Programmable Gate Array (FPGA) fully digital implementation has been used. A fault tolerant "six-leg" converter topology with one redundant leg and a Doubly Fed Induction Generator (DFIG) for WECS has also been studied [5]. The fault-detection scheme and the compensation algorithm have also been implemented into an FPGA target. By implementing a redundant leg, the applied control strategy remains the same for both healthy and faulty operation modes, because the converters topology remains a "six-leg" structure after the fault-detection and compensation.

Five-leg converter topology has already been proposed for drive applications such as independent control of two three-phase motors [6] or AC/AC supply of a three-phase induction machine [7]. It has been shown that this converter topology could give satisfactory results in such applications. However, in post-fault operation, the DC bus voltage value has been doubled to preserve the maximum power capability of the drive. However, doubling the current and voltage implies that the power switches ratings must be four times greater than those in healthy operation. Such high switch ratings results high additional costs. Accordingly, the

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authors have proposed to reduce the power level of the post-fault configuration to a suitable value and provide only the balanced operation of the drive. In this case, the power switches ratings could be the same as in normal operation. However in a WECS case, it is not possible to change instantaneously the active power level in post-fault operation by updating the reference rotational speed in controller. Because the electromechanical time constant of the wind turbine is much larger than the electric time constant of the DFIG [8]. In Ref. [9], a five-leg converter control has been studied for a WECS in normal operation mode. However, as far as WECS with DFIG is concerned, the applications of such a reconfigured “five-leg” converter in switch fault operation with the associated FPGA-based reconfigurable control have never been reported in the literature. Such a converter topology might be interesting and efficient for this purpose.

This paper proposes an FPGA-based reconfigurable control for “six-leg” fault tolerant converter topology without redundancy, which can be used in WECS with DFIG. The fault tolerant topology and the associated control give the possible switch failure fault tolerance capability. Compare to classical “six-leg” converter used in WECS with DFIG, the proposed fault tolerant converter requires three additional bidirectional devices. After switch fault detection and converter reconfiguration, the converter becomes a “five-leg” topology. Thus, the control strategy for “six-leg” configuration in healthy condition can no longer be applied to this “five-leg” structure and must be reconfigured as quickly as possible. For this purpose, a fast fault-detection method developed in Ref. [3] has been used. Moreover, in order to perform fast fault-detection and control reconfiguration, the entire digital control has been implemented into a single FPGA target [10]. The FPGA implementation offers many advantages: possibility of reducing the sampling period, insensitive to disturbance, the possibility of full integration of control system in a single control board and rapid reprogramming [11].

In the next section, the proposed converter topology has been presented. The proposed method that uses a common leg after the fault detection has been explained. Reconfigurations of converters in the cases of an open-circuit and short-circuit faults have also been discussed. After that, the reconfigurable control to switch from the classical control for a six-leg converter to the new control for the five-leg converter has been detailed. At last, experiments in healthy or faulty conditions using “FPGA in the Loop” hardware implementation have been presented and carefully discussed.

2. Fault tolerant six-leg converter topology without redundancy

2.1. Fault tolerant converter topology

The classical WECS, with a horizontal axis wind turbine and an indirect controlled 3 MW DFIG with Maximum Power Point Tracking (MPPT) and pitch controls has been used in this study [12,13]. The proposed fault tolerant WECS with DFIG, without power switch redundancy, is shown in Fig. 1. The power converter is based on the classical “six-leg” topology, which is composed by 12 semi-conductors (S_i and $S_{i'}$) and 12 anti-parallel diodes (D_i and $D_{i'}$), with $i = \{1, 2, 3, 4, 5, 6\}$.

Compared with the classical one, the proposed fault tolerant converter topology includes also fast active fuses (f_i and $f_{i'}$) and three additional current bidirectional switches T_k ($k = \{1, 2, 3\}$). After the fault occurrence and detection of a power switch, the reconfigured converter topology becomes a “five-leg” structure with a common leg shared by the Rotor Side Converter (RSC) and the Grid Side Converter (GSC). It should be noted that fast acting fuses are connected in series with each power switch in the proposed fault tolerant topology (Fig. 1). In the case of an open-circuit, the isolation is implemented by removing the gate signal from the switches of the faulty leg. In the case of a short-circuit, the faulty leg is isolated by the very fast acting fuses. The role of fuses and their selection criteria regarding corresponding drivers will be discussed later in this paper. In both cases, the isolation is implemented by removing the gate signals from the switches of the faulty leg. In summary, the fault compensation is achieved by the following steps:

- detection of the faulty leg,
- removing the control orders of the faulty leg,
- triggering the suited bidirectional switch T_k,
- adjust or not the DC bus voltage depending on the DFIG speed,
- changing the PWM control for both RSC and GSC,
- stopping the fault-detection scheme.

2.2. Common leg connection after fault detection

An equivalent circuit per phase for the RSC and the GSC is presented in Fig. 2. R_f and L_f are, respectively, the resistance and the

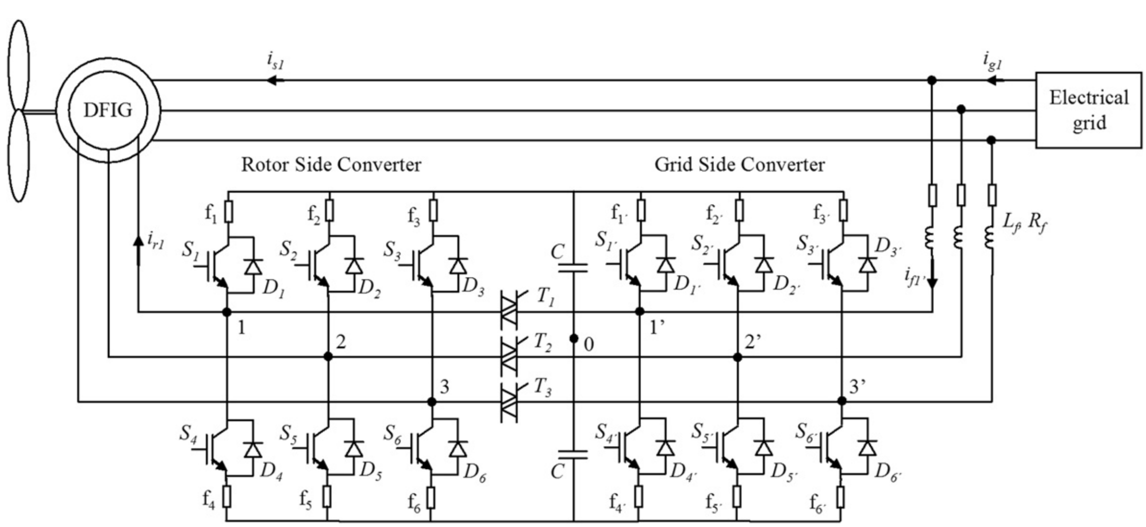

Fig. 1. Fault tolerant WECS with DFIG without power switch redundancy.