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Synthesis of lumped dual-frequency impedance transformers for complex loads using inverters

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ABSTRACT

Novel lumped dual-frequency impedance transformers (DFITs) for arbitrary frequency dependent complex loads (FDCLs) are synthesized using the concepts of capacitive and inductive inverters. Such a dual-frequency impedance transformer is constructed with one Pi-shaped lumped inverter and two shunt susceptance blocks at two sides, and get simplified after susceptance merging. The shunt susceptance blocks have specified susceptance values at two frequencies and are realized with lumped circuits of certain topologies. Design formulas of the DFITs are derived and are validated by two examples. Compared with a former technique, this method uses less lumped elements and provides one design freedom, so largest matching bandwidths can be achieved by comparing a series of possible designs.

1. Introduction

As more and more wireless communication standards are issued, microwave components, such as power amplifiers, power splitters and antennas are demanded to work on two or more frequency bands. As a key part of these devices, dual-frequency impedance transformer has attracted much research attention.

Dual-frequency impedance matching was firstly realized between real impedances using the structures such as commensurate two-section lines [1], L-shaped [2] and Pi-shaped [3] transmission line networks. As to arbitrary FDCLs, DFITs can be realized by cascading three sections of lines [4], by cascading two lines and a two-section stub [5], or by constructing a T-shaped network [6], etc. The above DFITs are distributed solutions with large dimensions especially at the low frequencies, whereas lumped solutions have smaller dimensions and are easier to be integrated into RFICs. A lumped DFIT between two real impedances is achieved by frequency transformation [7]. For FDCLs, although three topologies are proposed in [8], but only Pi-shaped topology containing three dual-frequency susceptance or reactance blocks can ensure realizing dual-frequency matching for arbitrary loads, at the expense of using many elements.

Although optimal dual-band impedance transformers have been designed by following classic wide-band matching theory [9], the loads are not arbitrary but constrained to be fixed topologies like RC circuit, and the circuits are complex. Practically, moderate matching bandwidths realized with less elements and simpler circuits are still preferred for dual-band telecommunication applications.

The concept of multi-mode inverter has been used in designing distributed multi-frequency impedance transformers [10], and is extended in this paper in realizing lumped DFITs, which use less elements than a former technique [8], and provide one design freedom. The novel DFITs can deal with arbitrary complex load, and the same topology can be extended for designing multi-frequency impedance transformers.

2. Topologies and synthesis theory of the DFITs

Fig. 1(a) and (b) are the basic topologies of two type DFITs, which are terminated by frequency-dependent complex loads: $Y_l = G_l + jB_l$. Each DFIT contains two shunt susceptance blocks and one J inverter realized using capacitive or inductive Pi-shaped network [11]. Here we take Fig. 1(a) as an example for analysis.

A J inverter of Fig. 1(a) is used to achieve the inverse of an admittance. Containing one positive capacitor C and two negative capacitors $-C$, the J inverter can work at any frequency, but with frequency-variant J value, and we can regard it as a multi-frequency inverter. At the specified two frequencies, the J values

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are as follows:

$$J(f_i)=\omega_i C \quad i=1,2 \tag{1}$$

Referring to Fig. 1(a), we have:

$$Y'_{in}(f_i)=Z'_l(f_i)(\omega_i C)^2 \quad i=1,2 \tag{2}$$

For achieving impedance matching, $Y'_{in}(f_i)$ must have a real part as matched admittance Y_0, so:

$$\mathrm{Re}(Y'_{in}(f_i))=\mathrm{Re}\left(\frac{(\omega_i C)^2}{G_l(f_i)+jB_l(f_i)+jB_{a1}(f_i)}\right)=Y_0\le\frac{(\omega_i C)^2}{G_l(f_i)} \quad i=1,2 \tag{3}$$

here $G_l(f_i)$ and $B_l(f_i)$ are the real and imaginary parts of the admittance of the load at the specified frequencies. The value of C can be chosen with certain freedom:

$$C\ge\max_{i=1,2}\sqrt{\frac{Y_0G_l(f_i)}{\omega_i^2}} \tag{4}$$

When the value of C is selected, from (3) we can derive $B_{a1}(f_i)$, which have two possible values:

$$B_{1a}(f_i)=\pm\sqrt{\frac{G_l(f_i)(\omega_i C)^2}{Y_0}-G_l^2(f_i)}-B_l(f_i) \quad i=1,2 \tag{5}$$

The shunt block jB_{a2} is used to compensate the imaginary part of $Y'_{in}(f_i)$, so:

$$B_{a2}(f_i)=-\mathrm{Im}\left(Z'_l(f_i)(\omega_i C)^2\right) \quad i=1,2 \tag{6}$$

The negative shunt capacitors cannot be directly implemented but can be absorbed by neighboring susceptances, and we get:

$$\{B_{at1}(f_i)=B_{a1}(f_i)-\omega_i C \quad i=1,2 \tag{7-1}$$

$$\{B_{at2}(f_i)=B_{a2}(f_i)-\omega_i C \quad i=1,2 \tag{7-2}$$

Following a similar analysis procedure, we get the design equations of DFIT of Fig. 1(b) as below:

$$L\le\min_{i=1,2}\sqrt{\frac{1}{Y_0G_l(f_i)\omega_i}} \tag{8-1}$$

$$B_{b1}(f_i)=\pm\sqrt{\frac{G_l(f_i)}{Y_0(\omega_i L)^2}-G_l^2(f_i)}-B_l(f_i) \quad i=1,2 \tag{8-2}$$

$$B_{b2}(f_i)=-\mathrm{Im}\left(Z'_l(f_i)/(\omega_i L)^2\right) \quad i=1,2 \tag{8-3}$$

$$B_{bt1}(f_i)=B_{b1}(f_i)+1/\omega_i L \quad i=1,2 \tag{8-4}$$

$$B_{bt2}(f_i)=B_{b2}(f_i)+1/\omega_i L \quad i=1,2 \tag{8-5}$$

Now the problem is to implement the shunt susceptance blocks of jB_{at1}, jB_{at2}, jB_{bt1} and jB_{bt2}. In Fig. 2 there are four lumped circuit

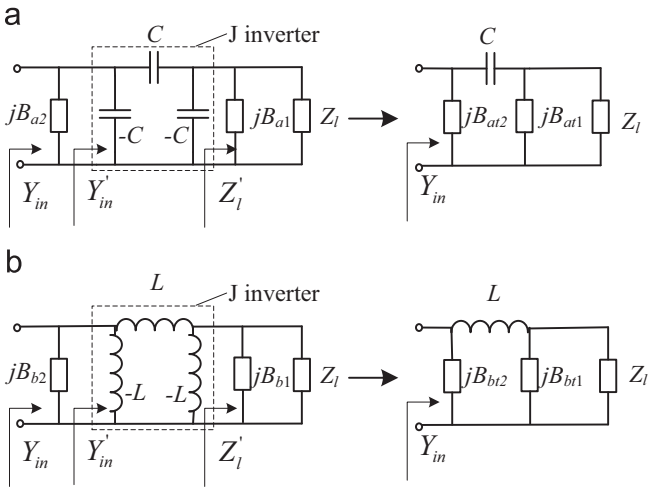

Fig. 1. Topologies of the proposed two types of DFITs. (a) Using capacitive J-inverter; (b) Using inductive J-inverter.

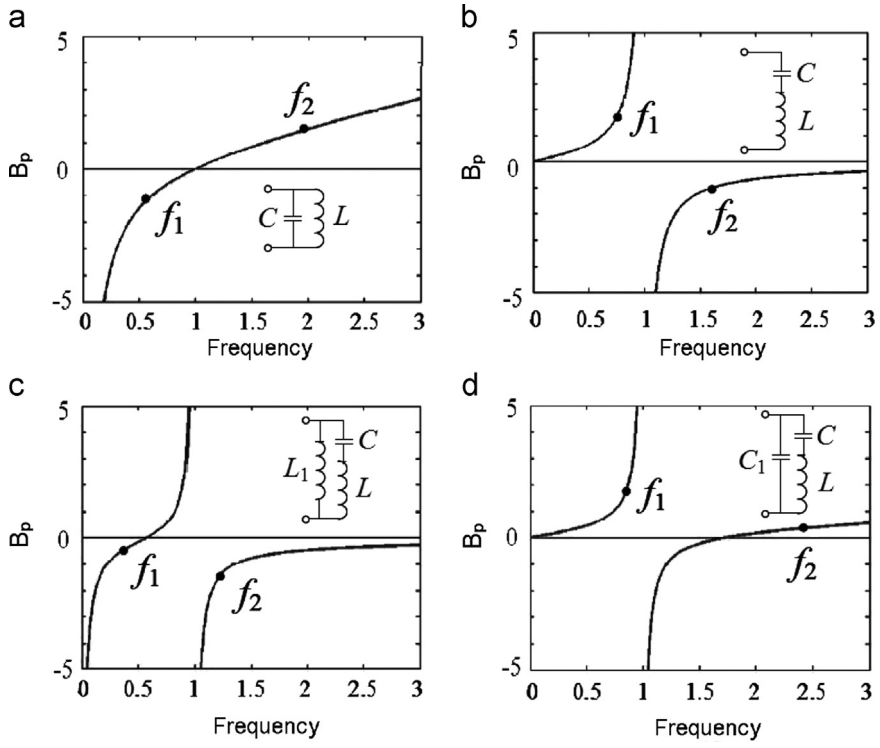

Fig. 2. Four types of lumped circuit blocks for realizing shunt susceptances: (a) $B_p(f_1)<0<B_p(f_2)$; (b) $B_p(f_1)>0>B_p(f_2)$; (c) $0>B_p(f_1)>B_p(f_2)$; (d) $B_p(f_1)>B_p(f_2)>0$.