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# Development and testing of a bidirectional distribution electronic power transformer model

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ABSTRACT

Transformer size can be significantly reduced by increasing the operating frequency, which may be achieved by means of power electronics converters installed as interfaces to the power frequency systems at both transformer sides. In this work, a model for a bidirectional high-frequency power electronic transformer is presented. Several case studies have been carried out in order to evaluate the behavior of the transformer under different operating conditions and test the impact on the power quality. The results show that the electronic power transformer, also known as solid-state transformer, not only matches the functions of a conventional power transformer, but also provides additional capabilities to mitigate dynamic power quality problems.

## 1. Introduction

Transformers are widely used in electric power systems to perform primary functions, such as voltage transformation and isolation. Since the size of a conventional copper-and-iron based transformer is inversely proportional to the operating frequency, an increase of this frequency would provide a higher utilization of the magnetic core and a reduction in transformer size [1].

The connection of distributed energy resources (i.e., distributed generation, storage devices) is raising new challenges. For instance, a high penetration of distributed generation at a low voltage (LV) distribution grid might force a power flow reversal across distribution transformers, which means that the LV distribution system may become a distributed generation source for the higher-level medium voltage (MV) grid [2].

Although the conventional transformer has been, and still is, the traditional link between end-users and the distribution network, the high-frequency electronic power transformer is foreseen as a fundamental component that might cope with many of the challenges of the future smart grid [3,4].

As compared to the conventional transformer, the electronic power transformer does not only reduce the size and eliminates oil but may also enhance the power quality performance. The list of new capabilities available to this new type of transformer includes voltage sag compensation, instantaneous voltage regulation, harmonic compensation, power factor correction, auto-balancing and variable-frequency output [5–11]. In addition, its control must allow the possibility of having bidirectional power flow and achieve the mitigation of faults and disturbances coming from both sides.

A model for a bidirectional distribution electronic power transformer (DEPT) is presented in this paper. The goal is to study its behavior under variable operating conditions and/or in presence of disturbances, located at both sides of the transformer.

The document is organized as follows. The description of the proposed bidirectional transformer and the simulation model are respectively presented in Sections II and III. The control strategies are presented in Section IV. The transformer model, implemented in Matlab/Simulink [12], has been tested under several dynamic and unbalanced conditions. Section V presents the test system used for benchmarking the DEPT model and some simulation results. Future development is discussed in Section VI.

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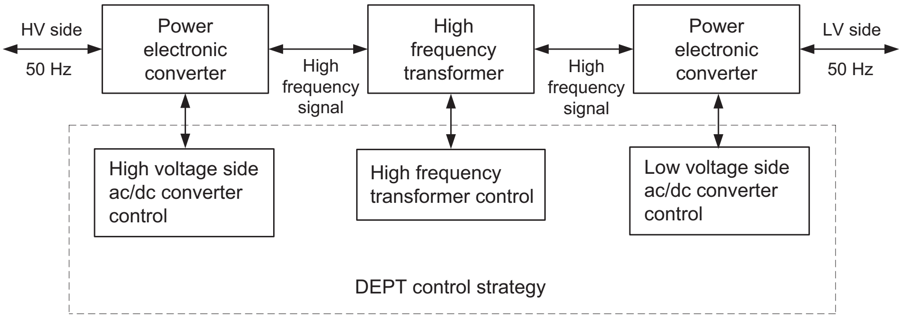

**Fig. 1.** DEPT control block diagram.

## 2. Description of the electronic power transformer

This section provides a brief overview of the circuit topology and working principles of the DEPT model selected for this study. A basic block diagram for the bidirectional DEPT and the corresponding control is shown in Fig. 1. It includes three parts: a high-voltage stage, an isolation stage, and a low-voltage stage [13]. Fig. 2 shows a detailed and feasible topology for each part of the DEPT. Although the new device can manage bidirectional power flow, in this paragraph, as a matter of explanation, the power is considered flowing from the HV side to the LV side. In such case, the input voltage at power frequency is first converted into dc voltage by the HV-side three-phase pulse width modulated (PWM) ac/dc converter, shown in Fig. 2a, working as rectifier in this case.

The isolation stage includes the high-frequency transformer, and the two corresponding HV- and LV-side H-bridge voltage source converters (VSC).

The HV-side converter, shown in Fig. 2b, converts the HV dc voltage into a high-frequency square-wave voltage applied to the primary of the high frequency transformer. In the secondary side, the transformed high-frequency square-wave signal is converted into a LV dc voltage by the LV-side converter. Finally, the LV-side three-phase PWM dc/ac converter, shown in Fig. 2c, works as inverter and provides the output power-frequency ac waveform from the low dc voltage.

The HV side (hereinafter known as input side) of the DEPT is intended to be coupled to a MV distribution system, while the LV side (hereinafter known as output side) is connected to a mixture of load and generation.

When the power flow comes from the secondary side, in case it is acting as generation, the transformer behavior is similar as described above. Basically, input and output stages swap functions.

In this work, conventional two-level converters have been used for all the converters. However, multilevel converters can be better suited for the HV side of the electronic power transformer [14–16]. The use of a HV-side multilevel topology will affect the switching strategy used with the present implementation, but it will not affect the control approach proposed in this work. Therefore, there is no need to change the controllers if the topology proposed in this work is replaced by a multilevel implementation, although each topology will need its corresponding switching strategy.

Finally, notice that some multilevel topologies need to keep balanced the dc-link capacitors voltage (as for example, the neutral-point-clamped topology). This task is usually carried out by the switching strategy, by taking advantage of the redundant switching states of the multilevel converter.

## 3. DEPT model

As shown in the previous section, the DEPT is divided in three different parts decoupled by two large intermediate dc-link capacitors ($C_{dc1}$ and $C_{dc2}$). No losses have been considered in the model, apart from the filter and transformer copper losses, represented by suitable series resistances. The simulation model for each part is presented in this section.

### 3.1. Input stage – high-voltage side front-end converter

The input stage is implemented by means of a three-phase PWM converter, which, in recent years, has gained popularity in various industry applications, such as renewable energy systems or power supply systems [17–19]. The *abc*-frame model for the PWM converter is as follows:

$$\frac{d}{dt}i_{i1} = -\frac{R_1}{L_1}i_{i1} - \frac{1}{L_1}(v_{i1o} - v_{N1o}) - \frac{1}{L_1}v_{i1grid} \qquad (1)$$

where $i \in a, b, c$; $i_{i1}$ are the HV side abc grid currents, $v_{i1o}$ are the HV side abc converter voltages (referred to a fictitious dc-link midpoint “o”), $v_{i1grid}$ are the HV side abc grid voltages (referred to the grid neutral point “N1”), $v_{N1o}$ is the HV grid neutral to the fictitious dc-link midpoint voltage, L$_1$ is the HV side filter inductance, and $R_1$ is the HV side filter resistance.

Each IGBT-diode pair in the converter shown in Fig. 2a can be considered as a simple switch defined by:

$$S_{ij} = \begin{cases} 1 & \text{when } i \text{ is connected to } j \\ 0 & \text{when } i \text{ is not connected to } j \end{cases} \qquad (2)$$

where $i \in \{a1, b1, c1\}$ and $j \in \{p1, n1\}$.

The ac lines ($a1$, $b1$, $c1$) cannot remain in open-circuit, because of the filter and wire inductances, therefore each ac line must be connected to any dc rail ($p1$, $n1$) at any time; this condition may be expressed as:

$$S_{ip1} + S_{in1} \geq 1 \qquad (3)$$

Similarly, the dc-link capacitor cannot be short-circuited by the switches action, resulting in

$$S_{ip1} + S_{in1} \leq 1 \qquad (4)$$

Merging (3) and (4) results in the following switch operation restriction:

$$S_{ip1} + S_{in1} = 1 \qquad (5)$$

By using (2) and (5), ac and dc variables in the converter presented in Fig. 2a can be easily linked

$$\begin{bmatrix} v_{a1o} \\ v_{b1o} \\ v_{c1o} \end{bmatrix} = \begin{bmatrix} S_{ap1} & S_{an1} \\ S_{bp1} & S_{bn1} \\ S_{cp1} & S_{cn1} \end{bmatrix} \cdot \begin{bmatrix} v_{p1} \\ v_{n1} \end{bmatrix} = [S] \cdot \begin{bmatrix} +v_{dc1}/2 \\ -v_{dc1}/2 \end{bmatrix} \qquad (6)$$