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A novel harmonic-free power factor corrector based on T-type APF with adaptive linear neural network (ADALINE) control

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ABSTRACT

A novel harmonic-free power factor correction (PFC) topology based on T-type active power filter (APF) is proposed in this paper. The proposed system has better stability characteristics compared to conventional shunt APF topologies and it is a natural filter for the non-linear load harmonic disturbances. The tuned passive filters are connected at the ac-side of the rectifier load, which are designed to provide fundamental reactive power compensation and eliminate majority of load harmonics in order to minimize the power rating and heat dissipation of the voltage source inverter (VSI). The control scheme is based on a decoupled state-space equations of the T-type APF using separate proportional-integral controllers in *d*-axis and *q*-axis of rotating reference frame synchronized with grid voltages, respectively. The fundamental components of load-side currents are feed-forwarded in the current control loop using two groups of synchronous frame adaptive linear neural networks (ADALINEs) to ensure a fast dynamic response. A proportional-integral controller is adopted in the outer voltage loop for balancing the active power flow of the dc-side capacitor of the VSI. The proposed power factor corrector topology is studied analytically and by simulation under various scenarios using Matlab/Simulink. The validity and effectiveness of the proposed topology as well as its control schemes are substantially confirmed by the simulation results.

1. Introduction

In recent years, power converters are widely used in industry as front-end rectifiers for ac-drive applications. These converters generate a large amount of characteristic harmonics and cause a low power factor, which deteriorate the power quality of electrical distribution systems. The harmonics travel upstream and cause voltage drop across the line impedance, resulting in instabilities and harmonic proliferation throughout the network. The simplest method to eliminate the characteristic harmonics and improve system power factor is to use passive filters tuned around the characteristic frequencies, such as 5th, 7th, 11th or 13th order harmonics. Whereas, passive filters are bulky, and they may detune with age, causes series or parallel resonance between line impedance and the passive components.

All the aforementioned drawbacks of passive filers can be overcome by using active power filers (APFs) [1–4] for harmonic and reactive power compensation. Normally, the shunt active power filters are used for current-source type non-linear load, such as six-pulse rectifier with inductive load at dc-side. And series active power filters are used for voltage-source type non-linear load, such as six-pulse rectifier with capacitive load at dc-side. Unlike passive filters, active filters have a tendency to destabilize at higher harmonic frequencies due to a broad bandwidth requirement of current control loop for shunt APF or voltage control loop for series APF [3]. Consequently, the shunt active filter is prone to instability

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when LC passive filters or power-factor correction capacitor banks are connected at the load side (downstream) from the point where the APF is connected [5,6]. Similarly, dual stability characteristics also exist for series APF. Besides, shunt APF with capacitive rectifier load shows another type of trend which causes the instability of overall system. The mechanism is that the currents generated by APF flow into the diode/thyristor rectifier or load side that presents low impedance, thus causing over-current of the load side and increasing the harmonic current significantly. To reduce such sort of undesired interactions, a series inductor between shunt APF and the load is inevitable. Otherwise, total harmonic compensation is not theoretically achievable in presence of low leakage inductance of the main supply transformer [5].

In order to overcome the stability problems of shunt active filter in case of compensating capacitive rectifier load, this paper proposes a new power factor corrector topology based on the T-type active power filter structure for harmonic and reactive compensation of six-pulse diode/thyristor converters, which exist in most of the front-end rectifier for ac drive applications. The proposed T-type active power filter is cascaded between the rectifier converter and the power distribution panel as the first power conversion stage. The tuned passive filter is shunt connected at the ac-side of the rectifier converter for the purpose of reducing the power rating of the voltage source inverter (VSI). This topology has the characteristic of decoupling the line impedance from the load impedance at higher frequencies, thus it has effective harmonic rejection capability at higher frequencies. The stability of the proposed system is ensured by reducing the controller bandwidth of the active T-type filter voltage source inverter (VSI).The presented topology has many advantages over the conventional shunt active power filters, such as: (a) total harmonic compensation can be implemented with simple control algorithm, (b) smaller bandwidth of sensors and controller, (c) it is immune to one cycle delay inherent in digital signal processor (DSP) or microcontroller implementation.

If the passive filer is designed to eliminate the majority of the dominant harmonics by presenting low impedance path and compensate the fundamental reactive power required by the non-linear load, the compensating current of voltage source inverter (VSI) can be minimized. The control objective of the proposed harmonic-free power factor corrector system is to achieve a near unity power factor (NUPF) or unity power factor (UPF) and no harmonic currents at the source side, depending on the selection of reference signals for the current loop controllers. In the proposed control scheme, both source side and load side currents are sensed using current transducers (CTs). The inner current loop is responsible for fast current tracking, using proportional-integral (PI) controllers in d-axis and q-axis rotating reference frame synchronized to the grid voltages by using a software phase-locked-loop (PLL). The proportional-integral controllers are implemented in d-axis and q-axis based on the decoupled state-space equations of the T-type active power filter. The load side dynamics are incorporated in the feed-forward loop by using synchronous frame adaptive linear neural networks (SADALINEs) [7–11] in d-axis and q-axis, respectively, for fast estimation the fundamental components of non-linear load currents. Besides, a separate proportional-integral (PI) controller is adopted in outer voltage loop for balancing the active power flow of the voltage source inverter. The proposed topology and its control schemes are evaluated by theoretical analysis and digital simulations under various scenarios. The effectiveness and validity of the proposed reference signal generation scheme is further proved by comparison with three well-known approaches, namely, low pass filter (LPF) approach, FFT/DFT approach and instantaneous reactive power theory (IRPT) approach.

2. System configuration of the proposed harmonic-free power factor corrector

Fig. 1 shows the circuit diagram and main components of the proposed power factor corrector topology based on T-type active power filter. This system is composed of three parts, conventional three-phase rectifier, a passive filter and a T-type active filter. The passive filter is used for reducing the power rating of voltage source inverter (VSI) in active T-type filter. It is tuned to eliminate the dominant harmonics by presenting a low-impedance path for the load current harmonics. The active

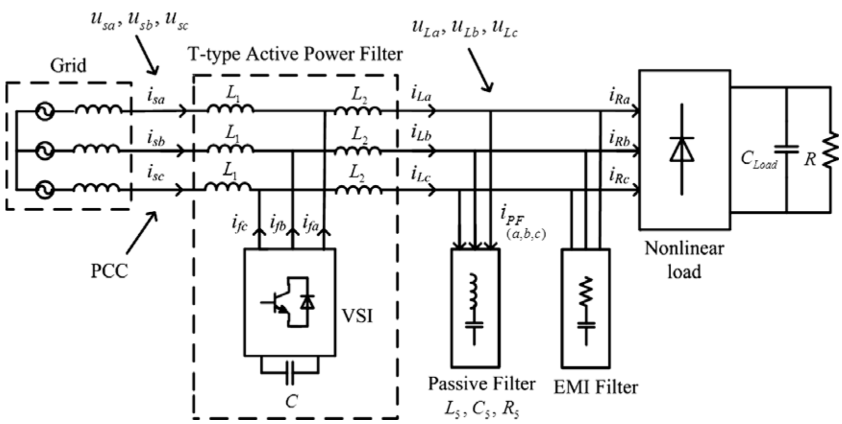

Fig. 1. Proposed harmonic-free power factor corrector topology based on T-type APF.