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Parameter estimation procedure for the equivalent circuit model of compact fluorescent lamps

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ABSTRACT

The spreading use of compact fluorescent lamps (CFLs) in utility distribution systems is leading to increased concerns over power quality because CFLs consume highly distorted currents, which may account for significant power consumption of distribution feeders. For this reason, CFL models and estimation procedures of CFL model parameters must be studied in order to predict CFL harmonic current emissions into networks. This paper describes estimation procedures of CFL model parameters and presents estimation algorithms based on least-square techniques and actual measurements. The estimation procedures are validated with extensive laboratory measurements.

1. Introduction

CFLs are small-power, energy-efficient lighting devices increasingly used in residential and commercial installations due to their low energy consumption and long useful life in comparison with incandescent lamps. CFLs consume highly distorted current waveforms, which can pose a harmonic issue because CFL power consumption of all residential and commercial customers in a power distribution system may be of the order of mW, causing unacceptable voltage distortion in distribution feeders [1–3].

For the above reason, CFL modeling is currently studied in the literature in order to assess CFL harmonic current injection and predict its impact on power quality [1,2,4–6]. In [1], supply voltage harmonic interaction in CFL harmonic currents is modeled using the concept of tensor analysis with phase dependence. In [2], CFL harmonic currents are introduced in power flow calculation with Norton equivalent circuits. In [4], CFL study is based on the CFL equivalent circuit without considering its ac equivalent resistance because it can lead to unrealistic infinite slopes in the ac current rising edge. In [5], the CFL equivalent circuit is improved by considering the ac equivalent resistance because it enhances the accuracy of the model at the expense of a slight increase in model complexity. In [6], CFL external behavior is modeled using a double-exponential function to characterize ac current waveform dependence on the supply voltage without considering the internal electric circuit. CFL parameter estimation procedures are also necessary to allow use of the previous models in harmonic studies but they have not been studied as extensively as CFL modeling. Little detailed information about CFL parameter values is available and only a few works deal with parameter estimation of the CFL equivalent circuit model [1,4,5,7]. In [1], typical dc capacitor values of either 4.7 μF or 10 μF are suggested for CFL modeling. In [4], a simple procedure for determining the parameters of the 120 V, 60 Hz CFL equivalent circuit model from limited information is described. In [5], a straightforward method for CFL parameter estimation using experimental measurements of the CFL supply voltage and ac consumed current is proposed. In [7], a range of typical values for estimation of CFL equivalent circuit components is presented. Among these works, only the study in [5] provides an accurate estimation of CFL equivalent circuit parameters, although these results can be improved with least-square algorithms. These algorithms are used in [8] for estimating the parameters of the CFL double-exponential model in [6]. Other studies deal with the estimation of other non-linear loads using least-square algorithms [9–11]. In particular, [9,10] investigate parameter estimation of single-phase rectifiers by analyzing several non-linear sets of equations.

This paper examines CFL parameter estimation by non-linear least-square procedures based on actual measurements and the CFL equivalent circuit model in [5]. These procedures are experimentally validated with two laboratory tests performed on 12 CFLs of different power ratings and trade names. From this study, a non-linear least-square procedure based on the minimization of the square error between the temporal samples of the CFL measured and simulated ac currents is finally proposed.

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Table 1
Rated values and tolerances of 450 V CFL capacitors.

	C (μF)								
	...	1	1.5	2.2	3.3	4.7	6.8	10	...
Tol. (%)	±1	±2	±3	±5	±10	±20	+50 −20	+80 −20	±100
Code	F	G	H	J	K	M	S	Z	P

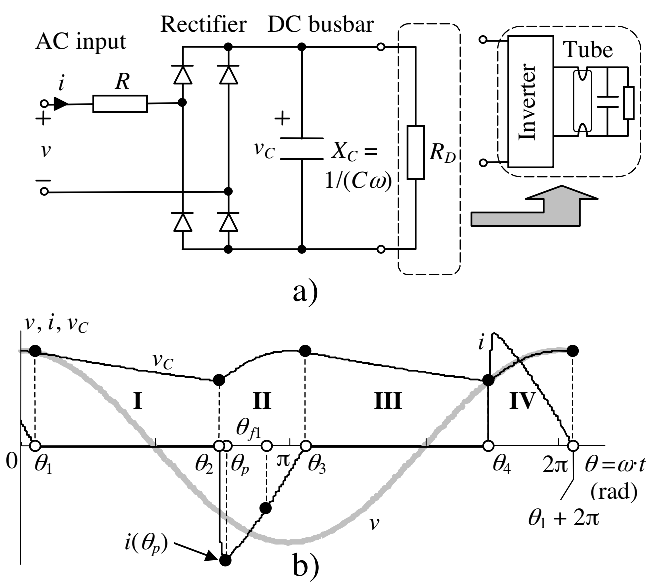

Fig. 1. CFL modeling: (a) CFL equivalent circuit. (b) Supply voltage v, ac current i and dc voltage v_C waveforms.

2. CFL modeling

The estimation procedures in this paper are based on the CFL equivalent circuit model in [5], which characterizes CFL behavior in "poor-average" harmonic spectrum category [1,2]. This CFL category covers most of the low-Watt (<25 W) CFL market share because the minimum power factor requirement of several Standards (e.g. ANSI C82.77-2002 and ENERGY STAR program requirements for CFLs) is 0.5 only [5]. CFLs with input power above 25 W are generally better because they must comply with the requirements for class C equipment of Standard IEC 61000-3-2. Fig. 1(a) illustrates the equivalent circuit of this category and Fig. 1(b) shows the typical ac current i and dc voltage v_C, which characterize CFL behavior where $\omega = 2\pi \cdot f$ and f is the fundamental frequency of the supply voltage v.

According to Fig. 1(a), the equivalent circuit is supplied from a non-sinusoidal "stiff" system and is composed of a diode bridge with an ac equivalent resistance R and a dc electrolytic capacitor C that feeds the inverter and the tube modeled as an equivalent resistance R_D [5]. The "stiff" supply system can be considered because CFL consumed power is much smaller than the short-circuit power of the supply system at the point of common coupling of the lamps. The ac equivalent resistance R represents the CFL input resistance R_{in} plus the contribution of the equivalent series resistance (ESR) of the dc electrolytic capacitor. ESR represents the capacitor ohmic losses and is characterized by the dissipation factor ($DF = \mathrm{ESR}/X_C$), which must be below 20% at low frequencies and capacitor rated voltages above 63 V [12]. The contribution to R of the rectifier diode dynamic resistance ($R_{\mathrm{Diode}} \approx 0.6\,\Omega$) and the equivalent parallel resistance of the dc electrolytic capacitor ($R_P \sim \mathrm{M}\Omega$) can be neglected. The CFL electrolytic capacitors directly influence the dc voltage ripple and, together with the load resistance R_D, determine the CFL harmonic current emissions [7]. These capacitors have standardized rated values and tolerances (permissible relative deviation from the rated value), which are identified with a letter code (see Table 1) [12]. The usual CFL capacitor size for 230 V systems is 4.7 or 10 μF [1,5].

According to Fig. 1(b), the ac current waveform starts with a time delay from the zero crossing of the supply voltage and has a very pronounced peak with a steep and a gentle slope of the ac current rising and falling edges, respectively. Two working modes can be distinguished in the CFL equivalent circuit operation [4,5]:

- Segments I ($\theta_1 < \theta < \theta_2$) and III ($\theta_3 < \theta < \theta_4$): The diodes are off and the capacitor discharges through the equivalent resistance R_D.
- Segments II ($\theta_2 < \theta < \theta_3$) and IV ($\theta_4 < \theta < \theta_1 + 2\pi$): The ac current i flows through the rectifier diodes, charging the capacitor and feeding the tube inverter.

The commutation angles (θ_1–θ_4), which define the CFL ac current and dc voltage in Fig. 1(b), must be determined by analyzing the circuit topologies of the above segments to characterize CFL behavior. Nevertheless, assuming half-wave symmetry, these angles verify that $\theta_{j+2} = \theta_j + \pi$ ($j = 1, 2$), and therefore only segments I and II must be studied. Thus, considering a non-sinusoidal supply voltage with K harmonics

$$v(\theta) = \sqrt{2}\sum_{k=1}^{K} Re\left\{V_k \cdot e^{jk\cdot\theta}\right\} = \sqrt{2}\sum_{k=1}^{K} Re\left\{\underline{V}_k \cdot e^{jk\cdot\theta}\right\}, \tag{1}$$

and the previous half-wave symmetry assumption, the analysis of Fig. 1(a) reveals that the equations characterizing the ac current and dc voltage waveforms of segments I and II are [5]

$$\begin{aligned} &(\mathrm{I}): \begin{cases} i^{(\mathrm{I})}(\theta) = 0 \\ v_C^{(\mathrm{I})}(\theta) = K_1 \cdot e^{-\frac{X_C}{R_D}\theta} \end{cases} \\ &(\mathrm{II}): \begin{cases} i^{(\mathrm{II})}(\theta) = \dfrac{K_2}{R} e^{-X_C\left(\frac{1}{R_D}+\frac{1}{R}\right)\theta} + \sqrt{2}\displaystyle\sum_{k=1}^{K} Re(\underline{I}_k \cdot e^{jk\theta}) \\ v_C^{(\mathrm{II})}(\theta) = K_2 \cdot e^{-X_C\left(\frac{1}{R_D}+\frac{1}{R}\right)\theta} + \sqrt{2}\displaystyle\sum_{k=1}^{K} Re(\underline{V}_{Ck} \cdot e^{jk\theta}) \end{cases}, \end{aligned} \tag{2}$$

where

$$\begin{aligned} &K_1 = \sqrt{2} \cdot e^{\frac{X_C}{R_D}\theta_1} \cdot \sum_{k=1}^{K} Re(\underline{V}_k \cdot e^{jk\theta_1}) \quad K_2 = -\sqrt{2} \cdot e^{X_C\left(\frac{1}{R_D}+\frac{1}{R}\right)\theta_2} \cdot \sum_{k=1}^{K} Re\left[(1+\underline{\beta}_k)\underline{V}_k \cdot e^{jk\theta_2}\right] \\ &\underline{I}_k = -\left(\frac{1}{R_D} + j\frac{k}{X_C}\right) \cdot \underline{V}_{Ck} \qquad \underline{V}_{Ck} = \underline{\beta}_k \cdot \underline{V}_k = \frac{jX_C}{k \cdot R - jX_C\left(\dfrac{R}{R_D}+1\right)} \cdot \underline{V}_k. \end{aligned} \tag{3}$$