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Modeling and multi-loop feedback control design of a SEPIC power factor corrector in single-phase rectifiers

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Abstract

In this paper, a comparative analysis of three multi-loops control schemes dedicated to the single ended primary inductance converter (SEPIC) power factor corrector (PFC) is presented. The first control technique uses a robust hysteresis current controller; the second control strategy consists of a frequency–domain linear design of regulators on the basis of a small-signal averaged model of the converter, whereas the third control design method uses the input/output feedback linearization approach applied on the large-signal state-space averaged model of the converter. In order to verify and compare the performance of all control schemes, numerical simulations are carried out on a switching-functions-based model of the converter, which is implemented using Matlab/Simulink. The control systems are tested under both rated and disturbed operating conditions. The systems performance is evaluated in terms of source current total harmonic distortion (THD), input power factor, and DC voltage regulation toward load disturbances.

Keywords: SEPIC; Power factor correction; THD; Rectifiers; Modeling; Control; Simulation

1. Introduction

High power quality is increasingly required for the power supply systems in order to comply with the international standards [7]. For this purpose, and especially for single-phase low power applications, switch-mode DC–DC converters, commonly known as power factor correction (PFC) circuits, are designed in order to ensure a high power factor at the mains side, and to emulate a purely resistive operation of the diode-bridge-based front-end rectifier [17].

Three families of non-isolated PFC circuits exist in the literature: the Buck [4], the Boost [21] and the Buck–Boost [6] topologies. The Buck topology is characterized by a low DC voltage at the output, but a high frequency commutated current at the input. Due to the discontinuous nature of the input current, the Buck converter has to be connected to an ultra-fast-recovery diode bridge when it is used as a PFC circuit. Although the low voltage stresses it may exhibit, a Buck PFC has a major drawback that is the necessity of a high frequency shunt filter to be inserted between the source and the diode bridge.

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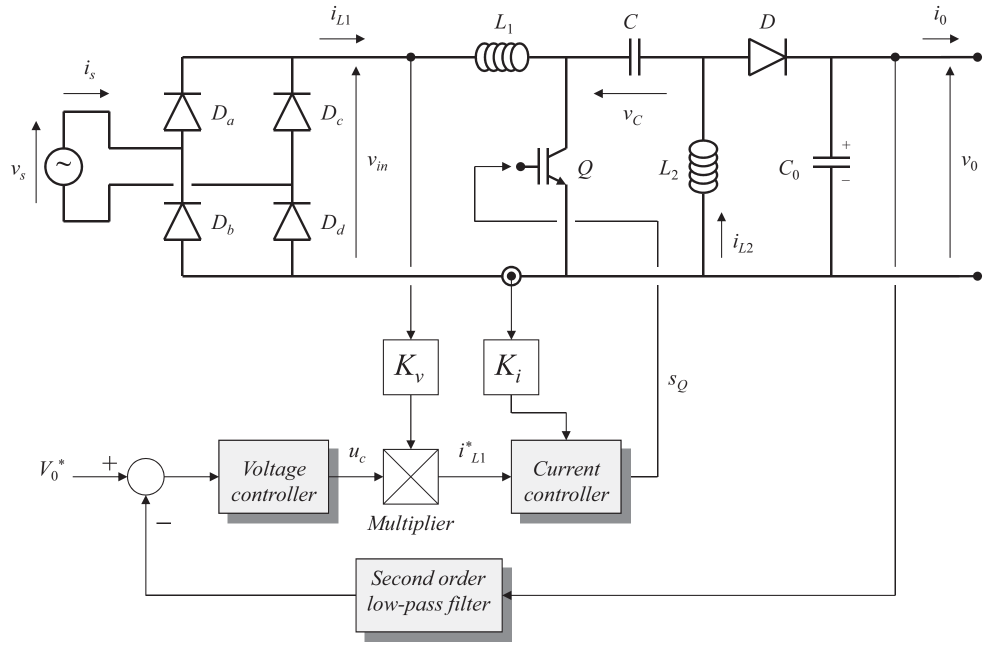

Fig. 1. Buck–Boost SEPIC power factor correction circuit and its control system.

On the other hand, the Boost-type topology presents a smoothly varying input current (due to the presence of a filtering inductor), but a relatively high DC-bus voltage (at least the peak value of the source voltage) that may cause over-voltage stresses on the switches. In addition, and contrarily to the Buck PFC, the front-end diode bridge operates in continuous current mode at the mains frequency (50 or 60 Hz) and, therefore, the presence of a high-frequency filter at the AC-side is no more necessary.

The third family of PFC concerns Buck–Boost combinations, in which the most suitable topologies for power factor correction are the Cùk converter [3,5,15,19] and the single ended primary inductance converter (SEPIC) [1,2,8,12–16,20]. These two converters differ from each other at the output stage, where the free-wheel diode and the output inductor are permutated, and the polarity of the output voltage is inverted. In both cases, the DC voltage delivered at the output can vary theoretically between zero and an infinite value.

In this paper, a SEPIC-type PFC circuit is adopted for improving the power factor at the input side of a single-phase diode rectifier, as described in Fig. 1. The main switch is controlled by a multiple-loops control scheme in order to ensure a line current wave-shaping and a DC load voltage regulation.

Three methods are considered for the design of the control scheme. The first uses a robust hysteresis current controller [11]; the second uses the classical frequency–domain linear design approach [10], whereas the third is based mainly on the input/output feedback linearization technique [9,18]. The performance of all considered control schemes is then analyzed through numerical simulations by using the Matlab/Simulink tool. For this purpose, a general-case switching-function-based mathematical model of the converter is implemented, and each control process is launched under varying operating conditions in order to test successively its steady-state characteristics and voltage regulation ability.

2. Averaged model of the converter

Referring to [11], the state-space averaged model of the converter operating in continuous current mode (CCM) and continuous voltage mode (CVM) is given by system (1), where $d(t)$ denotes the duty cycle of switch Q, and R_0 represents the DC load. Note that, in CCM/CVM operation, it is assumed that the conditions $(i_{L1}+i_{L2})>0$ and $v_C>0$ always stand; these assumptions are justified by a suitable choice of inductor L_2 and capacitor C. Moreover, in unity power factor (UPF) operation, the current i_{L1} is mainly in continuous mode, and would be only locally in discontinuous