

## Accepted Manuscript

Two-level Caches Tuning Technique for Energy Consumption in Reconfigurable Embedded MPSoC

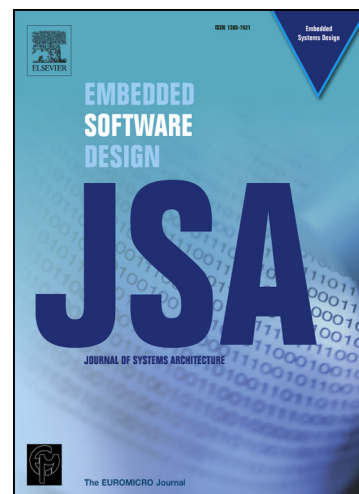
A. Bengueddach, B. Senouci, S. Niar, B. Beldjilali

PII: S1383-7621(13)00099-4

DOI: <http://dx.doi.org/10.1016/j.sysarc.2013.05.018>

Reference: SYSARC 1132

To appear in: *Journal of Systems Architecture*



Please cite this article as: A. Bengueddach, B. Senouci, S. Niar, B. Beldjilali, Two-level Caches Tuning Technique for Energy Consumption in Reconfigurable Embedded MPSoC, *Journal of Systems Architecture* (2013), doi: <http://dx.doi.org/10.1016/j.sysarc.2013.05.018>

This is a PDF file of an unedited manuscript that has been accepted for publication. As a service to our customers we are providing this early version of the manuscript. The manuscript will undergo copyediting, typesetting, and review of the resulting proof before it is published in its final form. Please note that during the production process errors may be discovered which could affect the content, and all legal disclaimers that apply to the journal pertain.



## Two-level Caches Tuning Technique for Energy Consumption in Reconfigurable Embedded MPSoC

A.Bengueddach<sup>a,b</sup>, B.Senouci<sup>b</sup>, S.Niar<sup>b</sup>, and B.Beldjilali<sup>a</sup>

<sup>a</sup> University of Oran, Department of Computer Science, BP 1524, El-M'Naouer, Algeria

<sup>b</sup> University of Valenciennes Hainaut-Cambrésis ISTV2- Le Mont Houy, LAMIH-CNRS UMR, 59313 Valenciennes Cedex9, France

**Abstract-** *In order to meet the ever-increasing computing requirement in the embedded market, multiprocessor chips were proposed as the best way out. In this work we investigate the energy consumption in these embedded MPSoC systems. One of the efficient solutions to reduce the energy consumption is to reconfigure the cache memories. This approach was applied for one cache level /one processor architecture, but has not yet been investigated for multiprocessor architecture with two level caches. The main contribution of this paper is to explore two level caches (L1/L2) multiprocessor architecture by estimating the energy consumption. Using a simulation platform, we first built a multiprocessor architecture, and then we propose a new algorithm that tunes the two-level cache memory hierarchy (L1 & L2). The tuning caches approach is based on three parameters: cache size, line size, and associativity. To find the best cache configuration, the application is divided into several execution intervals. And then, for each interval, we generate the best cache configuration; Finally, the approach is validated using a set of open source benchmarks; Spec2006, Splash-2, MediaBench and we discuss the performance in terms of speedup and energy reduction.*

**Keywords:** *Embedded system, MPSoC, Cache memories, Reconfigurable architecture, Energy consumption, Optimization*

متن کامل مقاله

دریافت فوری ←

**ISI**Articles

مرجع مقالات تخصصی ایران

- ✓ امکان دانلود نسخه تمام متن مقالات انگلیسی
- ✓ امکان دانلود نسخه ترجمه شده مقالات
- ✓ پذیرش سفارش ترجمه تخصصی
- ✓ امکان جستجو در آرشیو جامعی از صدها موضوع و هزاران مقاله
- ✓ امکان دانلود رایگان ۲ صفحه اول هر مقاله
- ✓ امکان پرداخت اینترنتی با کلیه کارت های عضو شتاب
- ✓ دانلود فوری مقاله پس از پرداخت آنلاین
- ✓ پشتیبانی کامل خرید با بهره مندی از سیستم هوشمند رهگیری سفارشات