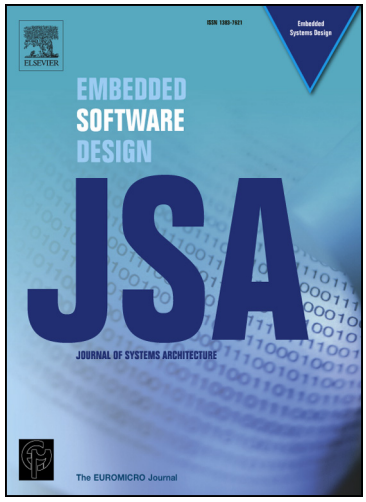

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Two-level Caches Tuning Technique for Energy Consumption in Reconfigurable Embedded MPSoC

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Abstract- *In order to meet the ever-increasing computing requirement in the embedded market, multiprocessor chips were proposed as the best way out. In this work we investigate the energy consumption in these embedded MPSoC systems. One of the efficient solutions to reduce the energy consumption is to reconfigure the cache memories. This approach was applied for one cache level /one processor architecture, but has not yet been investigated for multiprocessor architecture with two level caches. The main contribution of this paper is to explore two level caches (L1/L2) multiprocessor architecture by estimating the energy consumption. Using a simulation platform, we first built a multiprocessor architecture, and then we propose a new algorithm that tunes the two-level cache memory hierarchy (L1 & L2). The tuning caches approach is based on three parameters: cache size, line size, and associativity. To find the best cache configuration, the application is divided into several execution intervals. And then, for each interval, we generate the best cache configuration; Finally, the approach is validated using a set of open source benchmarks; Spec2006, Splash-2, MediaBench and we discuss the performance in terms of speedup and energy reduction.*

Keywords: *Embedded system, MPSoC, Cache memories, Reconfigurable architecture, Energy consumption, Optimization*