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Enabling design and simulation of massive parallel nanoarchitectures

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HIGHLIGHTS

- We conceive a tool for enabling the design and simulation of parallel nanoarchitectures.
- We develop specific algorithms to design layout of circuits based on silicon nanoarrays.
- We enable the fast simulation of circuits based on nanoarrays at behavioral level.
- We extract spice-equivalent netlists of circuits for physical level simulation.
- We include in algorithms and simulation device and interconnects models and/or measurements.

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ABSTRACT

A common element in emerging nanotechnologies is the increasing complexity of the problems to face when attempting the design phase, because issues related to technology, specific application and architecture must be evaluated simultaneously. In several cases faced problems are known, but require a fresh re-think on the basis of different constraints not enforced by standard design tools.

Among the emerging nanotechnologies, the two-dimensional structures based on nanowire arrays is promising in particular for massively parallel architectures. Several studies have been proposed on the exploration of the space of architectural solutions, but only a few derived high-level information from the results of an extended and reliable characterization of low-level structures.

The tool we present is of aid in the design of circuits based on nanotechnologies, here discussed in the specific case of nanowire arrays, as best candidate for massively parallel architectures. It enables the designer to start from a standard High-level Description Languages (HDLs), inherits constraints at physical level and applies them when organizing the physical implementation of the circuit elements and of their connections. It provides a complete simulation environment with two levels of refinement. One for DC analysis using a fast engine based on a simple switch level model. The other for obtaining transient performance based on automatic extraction of circuit parasitics, on detailed device (nanowire-FET) information derived by experiments or by existing accurate models, and on spice-level modeling of the nanoarray. Results about the method used for the design and simulation of circuits based on nanowire-FET and nanoarray will be presented.

1. Introduction

The remarkably successful era in computing, where Moore's Law reigns and processing power per dollar doubles every year, is approaching its end. Many attempts to keep up according to Moore's law have been put forward. Among them there is massive parallelism. Actually, parallel computation has been subject of interest and driving topic up to the development of integrated architectures. It is now even more a reality with multiprocessor systems, thanks to the integration capabilities reached by scaled technologies. However, even though parallelism levels now feasible are more sizable than ever, they allow to achieve only a tiny portion of what could really be faced in certain breakthrough applications (i.e. biological related processing in medicine [10]). Thus, even though research and technology is expected to greatly improve in this field during the following years, the predicted limits of CMOS technology [17,34] will prevent substantial revolutions in the amount of information that can be processed in parallel.

Hence, the new era of nanoelectronics is on the horizon, with ever smaller devices and higher densities [18]. Different nanostructures have been recently explored [25], however some of them will be rejected on account of the feasibility [16,35,14]. For what concerns massive parallelism, nanowire arrays [21,38,9], organized in matrices [22], which allow the creation of active nanodevices (diodes and FETs) in their crosspoints [15], have been proposed. These structures are generally organized in two-dimensional tiled arrays. In particular, nanoscale programmable

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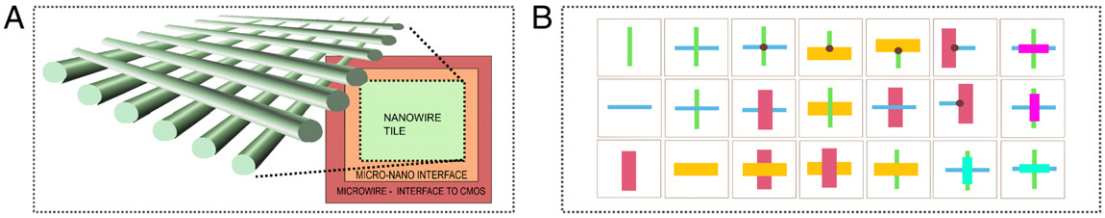

Fig. 1. (A) Generic organization of a nanoarray fabric structure: the structure requires interface to the external world, a system of interconnects both based on micro and nanowires, and the array of nanowires. (B) Different cross points (sub-tiles) composing the design if the focus is on an inner element of the matrix; elements can be microwires (bigger rectangles), nanowires (smaller rectangles), crossing among those sub-elements without or with contact (case with the small dot), nanowire FET transistors of N-type or P-type (represented by different colors here in the right column). (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

logic arrays, e.g. nanoPLA [7], or molecular/nanowire array, e.g. CMOL [20], have been investigated. NanoASICs (NASICs) designs have been indicated as a valid way to reach denser designs with better fabric exploitation and efficient cascading of circuits with respect to general-purpose programmable fabrics (PLAs) [23,26,31]. Some authors [27,28] proposed these structures for an optimal deployment of massively parallel architectures in specific applications, like cellular neural networks or image processors. Nevertheless, despite their promising characteristics, such structures have to deal with not negligible defect rates [32], mainly on account of critical manufacturing processes at nanoscale level. Defect tolerant techniques proposed for nanoscale arrays [5,24,39,1], showed the importance of faults analysis and fault techniques application in nanoarray-based structures.

Nanotechnologies in general represent an emerging field of study in which many questions are open. For example, the maximum density of devices obtainable after solving all the problems of reliability is still not known, neither which nanoarchitecture is best suited for a particular type of application. Epoch-making changing brings new challenges into play. New devices solicit the development of novel fabrication and integration approaches, novel simulation methods, and novel architectures to take full advantages from their potentialities. Moreover, design tools able to capture the specificities of these technologies are required, to explore the space of possible solutions, and to validate the proposed circuits and architectures. Hence, researchers need to revise the methodologies and design tools involved.

We propose a methodology to approach the above mentioned issues included in a tool we are developing: ToPoliNano (after Torino Politecnico Nanotech design tool). Even though not mature as an industrial level tool might be, the essential steps enabling the design and characterization of nanoarray based circuits are already implemented and are here presented. Starting from a VHDL circuit description, ToPoliNano can aim at different disruptive nanotechnologies (Nanoarray-based circuits as a possible example, as in Fig. 1(A), but not limited to), to place and route circuits on a low-level floorplan (please, see later section for details) and then to simulate it, in an integrated fashion, at both switch level and device level.

The aim of this tool is to analyze complex systems based on emerging electronic nanotechnologies. The study was specifically focused on the assessment of dimensions, performance, power consumption and, as a consequence, in developing optimized architectures. The ability to base its high level analysis of complex structures onto low-level information is a key aspect of ToPoliNano. This low-level information is derived from actual device technology, circuit topology and circuit layout post-placement parasitic extraction, in an efficient way. The expected overall result is, thus, an accurate characterization of the design, based on detailed technological parameters and device-level simulation results. The paper is organized as follows: previous work in the field and our case study structure are exposed Section 2; the general organization and features of ToPoliNano software are described in Section 3; its low-level floorplanning capabilities and related results are shown in Section 4; logic simulation and results are reported in Section 5; timing simulation are faced in Section 6.

2. Previous works and case study structure

Circuits based on nanoarrays have been largely investigated in the last years [16,32,7,20,31]. Their main attractive features are the high theoretical density of devices that can be obtained, the high frequency of operation, the low power consumption [10], and the possibility of being integrated with CMOS structures. However, the detailed study of circuits and architectures, considering at the same time device density, device defectiveness, power consumption, frequency of operation, etc., appears critical, on account of the interdependence of the obtained results. The assessment of main parameters affecting the feasibility of an architecture and its performance plays a fundamental role, in order to establish the priority in actions to be undertaken in a given technology and to identify the key aspects to be further investigated. Authors in [30,37] give an important overview of a possible architecture based on the regular composition of variably sized NASIC tiles, and this kind of exploration is essential towards a real implementation. Actually, the second and natural step in this method is the possibility to evaluate the effect of the modification of a transistor's technological parameter on the performance of a realistic circuit, as proposed in [30]. To be consistent, a third step should be undertaken, based on three main points. (i) The actual layout of the circuits, after all the constraints of placement and routing have been taken into account together with all the device and interconnects parasitics, has to be considered in the performance evaluation to reduce over or under estimation. (ii) This evaluation should be executed easily and if possible automated in order to allow the architect to make his own analysis. Moreover, (iii) a different resolution in terms of accuracy should be available, to enable evaluation speed on one side or accurate device level analysis on the other side, according to the designer needs. This third step is the one we are proposing with our method.

Besides the benefits of these technologies listed before, there is research interest about the importance of handling the high defectiveness of these structures, which has been investigated also in [32,19,24,1]. Different techniques of fault tolerance have been applied to these fabrics; in the form of the so-called built-in type, either through the reconfiguration of the fabrics. The defectiveness of these nanofabrics is a delicate point to be treated, because it is much higher than in the CMOS case. High defect rates are likely to considerably reduce the advantage in terms of maximum device density that can be reached, after the implementation of effective fault tolerance techniques. One evident problem underlined by the literature is the reduced availability of design and simulation tools expressly focused on the detailed design and simulation of these structures. One system level approach (the first step) has