

Caliper rule based ADC architectures

Roberto Lojacono *

Università di Roma "Tor Vergata", Dip. DIE, Viale del Politecnico, 1, 00133 Roma, Italy

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Abstract

In this paper, a new kind of architectures for the full-flash or subranging Analogue to Digital Converters (ADC's) is presented. To describe these architectures and explain the intrinsic conversion procedure, we refer to a technique, already presented by the author, which improves the accuracy of a measurement system. This technique is based on the arithmetic of the integer numbers in finite fields and include, as a particular case, the well known "caliper rule". The said technique is recalled and explained by using some simple measurement examples, in particular length, time and mass measurements. Then the technique is applied to the full-flash and subranging ADC architectures, greatly reducing the number of the resistors necessary to generate the voltage reference scale. Indeed, the required resistors for a n -bits conversion word length are reduced from 2^n to about $3 * 2^{n/2}$. This reduction and the particular comparison method involved in the theory allow the realization of full-flash architectures having large word lengths.

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1. Introduction

A traditional full-flash Analogue to Digital Converter (ADC) compares the input voltage with an internal reference voltage scale. This scale is realized driving a series of a great number of resistors, namely 2^n if n is the required word length, by a suitable voltage reference source. The number of resistors limits the practical implementation of these converters to 10 bits or minus. Also the most used subranging architectures, realized having the main purpose of reducing the number of comparators, require the same voltage reference scale and suffer

the same problem. Indeed the allocation of a great number of resistors into a single chip creates a lot of problems.

Random mismatch between monolithically integrated resistors is inversely proportional to the square root of their area while systematic mismatch due to process gradients increases with their area and separation. For a BiCMOS process, total resistor area should be less than about $10,000 \mu\text{m}^2$ to avoid gradient errors [1]. On the other hand, individual resistor areas must be well over $100 \mu\text{m}^2$ to obtain low random error. The resistor area versus matching trade-off is such that good matching of many resistors covering an area of the order of a square millimeter cannot be obtained if only first-order gradients are cancelled [2]. These constraints

* Tel.: +39 06 72597494; fax: +39 06 2020519.

E-mail address: lojacono@uniroma2.it

discourage the design of large word length full-flash ADC's.

This paper presents a new kind of architecture in which the reference voltage steps are realized by a technique derived from a particular case of a theory, here recalled and explained, which corresponds to the caliper rule. This technique implements a “virtual” fine reference voltage scale obtained by comparison between two scales having coarse steps. In this way the required resistors for a n -bits conversion word length are reduced to $3 * 2^{n/2}$. This reduction and the particular comparison method involved in the theory allow the realization of full-flash architectures having large word lengths.

2. Recall of the underlying theory

2.1. Some remarks

The accuracy of a measurement system is a feature which depends on some characteristics of the system. As an abrupt simplification we can consider:

- (a) the chosen measurement method;
- (b) the goodness of the whole involved hardware;
- (c) the smallest division of the scale;
- (d) the attention of the operator.

Here we fix the attention over the scales. Often the smallest division of the scale is related to the system possibilities: a more small division would not reduce the uncertainty related to the chosen measuring method and its implementation. In a simple length measurement procedure, based on hand made alignments e.g. using a simple meter divided by a scale, it is clear that the uncertainty of the measure cannot be reduced by reducing the smallest division of the scale well below the uncertainty of the hand made alignment.

But, in other cases, the smallest division of the scale is determined by different constraints: the realization of small scale divisions can be difficult or its observation can become unpractical.

In a time measurement, the smallest time interval which can be resolved by a clock correspond commonly to the period of the reference periodic physical phenomenon. That is, in a mechanical clock the period of the oscillating pendulum or of a mass-spring system or, in an electronic clock, the period of a vibrating quartz plate. Indeed, a partition of the said period becomes difficult.

We find an analogue situation in the case of mass measures. Usually, a pair of scales is furnished together with a set of reference masses and the order of the obtainable accuracy is related to the smallest mass of the given set. This smallest mass is chosen considering practical usage conveniences while the balance equipment can perform more small comparisons.

In this cases, when the intrinsic possibilities of the measurement system are not fully exploited, an introduction of a comparison between two or more scales can be very useful, as will be shown in the following.

2.2. Underlying theory: summary

The basic theory which underlies the proposed architecture was already proposed but briefly described by the author in two short congress communications [3,4]. Here are widely reported, for the sake of clarity, the useful features of this theory which are proposed for a generic improvement of the accuracy but can give also other advantages. The proposed improved measurement system make use of a comparison between “scales”. The said comparison between the scales determines a “virtual unit” that not exists physically but determines the available accuracy of the system [3]. This unit is referred in the following as “basic unit” (BU) of the measurement system under consideration. We consider here N scales of the type ϕ^1 [5], i.e. scales which have the same origin but different steps $u_i, i = 1, 2, \dots, N$ that have prime values in terms of BU.

2.3. Underlying theory: explanation

This explanation refers to length measurements but the theory can be applied to any physical quantity.

Suppose that to perform the length measurements we have available some physical segments having unknown lengths $u_i, i = 1, 2, \dots, N$ and the property that a multiple or a sub multiple of u_i cannot “correspond”, in terms of our available accuracy, to u_j , for all the i, j . The expression “prime each other” cannot be used here because the values of the lengths are still unknown. By iteratively reporting these lengths over a straight line we can create a set of scales, of the type ϕ^1 , following the notation given in [5], i.e. having the same origin but different steps. Let $n_i, i = 1, \dots, N$ be the integer

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