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Testing Low Voltage Ride Through capabilities of solar inverters

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ABSTRACT

The increase in the rated power of PV inverters has brought with it new requirements, such as Low Voltage Ride Through and reactive power compensation. Field tests in PV plants are too expensive in terms of production losses, and therefore laboratory tests have become a simple, flexible and inexpensive alternative. In this paper, a 500 kW test bench for testing solar inverters has been developed. The test bench is based on two inverters connected back-to-back. One of them acts as a controlled voltage source while the other is the inverter under test. The DC link is fed by a diode rectifier which only compensates for the power losses of all the elements in the test bench. With this test bench, Low Voltage Ride Through performance of a 500 kW solar inverter can be completely tested at full load. The results presented meet the requirements of the German BDEW standard.

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1. Introduction

Photovoltaic generation of electrical energy is now a reality. Thousands of photovoltaic plants throughout the world have been constructed in the last decade or two. Countries like Germany, Japan, the USA, Italy, Spain and China have several GW of installed capacity and targets for 2015 and 2020 are being revised and increased, as is the case of China, with 21 GW [1]. Most of the plants have small inverters (less than 100 kW). This usually yields plants with a lot of inverters. There are cases of small plants with a huge numbers of inverters, such as two hundred 5 kW inverters for a 1 MW plant [2] or one thousand 5 kW inverters for a 5 MW plant [3]. The consequences are clear for installation, maintenance, efficiency, monitoring and plant operation issues. Thus, there is a trend towards bigger photovoltaic inverters, 500 kW being one of the preferred sizes and, with this increase in size, new requirements must be met, like Low Voltage Ride Through (LVRT) or anti-islanding issues [4–11]. The objective of LVRT capability is to avoid a high loss of power in the case of a voltage dip in the grid, usually caused by faults. This was the case for wind farms until recently. The LVRT capability of wind generators could be tested on a single turbine in a wind farm which typically caused less than 5% power reduction and thus minimized the influence on wind farm performance [12,13]. However, this is not the case in PV plants, which have lower rated power than wind farms and where the cost of a field test would exceed reasonable values, reaching up to 25% power reduction during tests. In fact, some standards take this matter into account and allow the use of a laboratory test bench to test inverter performance [4,5,7,8].

Most of these standards were developed for wind energy integration and are being adapted for PV plants, mainly depending on the level of penetration in each country. Studies comparing different grid codes for wind energy were done [14–17] and can be used as a reference for photovoltaic energy. In Europe, countries like Germany or Spain have adapted their grid codes for PV plants [5,18]. Italy has recently released a new version of the grid code for distributed generation systems, explicitly including PV [7], including a new requirement for a two-phase sag at the HV level of the transformer (so called pseudo single-phase sag), but this discussion is out of the scope of the paper. Based on the ENTSO network code [19] and on the European Commission report [20], the next countries to follow the adaptation of their grid codes for PV plants must be France, Czech Republic and United Kingdom, with the goal to prove that PV is now a mature technology. In North America, in the USA, the North American Electric Reliability Corporation has recently approved the PRC-024-1 [6], which includes LVRT curves. In Canada, the Hydro-Quebec standard [9] is the reference since 2009. The case of China is slightly different because the LVRT requirement for wind turbines was recently approved [11,21,17], but as the growth in PV installed capacity is very high [1], it is probable that the adaptation for PV plants comes soon. In all cases, the voltage profiles for the sags are all very similar between different grid codes, with small changes in the remaining voltage and the duration, as is shown below for the case of the BDEW grid code.

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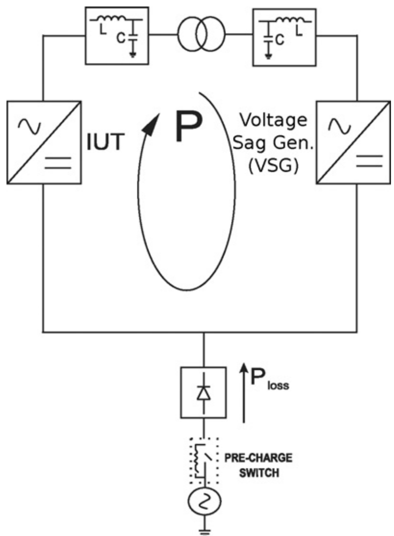

Fig. 1. One-line circuit of the test bench.

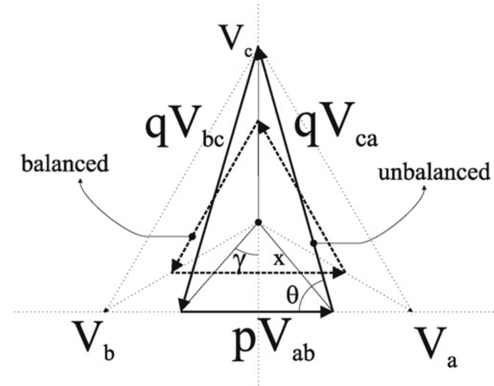

Fig. 2. Voltage phasors in a three-phase system: normal operation (dotted lines), three-phase sag (dashed lines) and unbalanced sag (bold lines).

In addition, LVRT field tests usually take a long time to be completed because they depend on weather conditions. Tests must be carried out at certain power levels, typically low-, medium- and full-load tests, which for wind energy depend on wind speed and for photovoltaic energy on irradiance and temperature. This implies a waiting time of several hours or even days.

These kinds of test benches are usually based on power electronic devices [22–24] as they provide high flexibility and high efficiency, and are a key element in current renewable energy systems and in the future smart grids [25,26]. As stated in [27], the reason a prototype is built is to demonstrate the functionality of a concept, although it may not have the actual size or power. The case of LVRT tests is special, because full-load tests are required by grid codes, but these have major drawbacks, as mentioned above. Moreover, when a voltage sag is generated in situ at power plants such as wind farms or PV plants, a high current is drawn from the grid because the sag is in fact a low impedance short circuit at the point of common connection (PCC) [28]. The proposed LVRT test bench allows rated power tests in a laboratory rig while the effect on the inverter under test remains the same.

2. Description of the test bench

The topology of the test bench is shown in Fig. 1, where the following components can be identified: (a) the inverter under test (IUT), a solar inverter with LVRT capability; (b) the AC source (voltage sag generator, VSG), a 550 kW voltage controlled inverter with a LC output filter, which can generate different voltage sag profiles at any load levels; (c) a diode rectifier to compensate for power losses of the entire test bench.

In this test bench, DC voltage is obtained by rectification of a 400 V AC grid voltage by means of a diode rectifier. The diode rectifier was sized to cope with the power losses of all components, in total less than 40 kW. The voltage sag generator is a voltage source inverter with a LC output filter. It has an open-loop voltage control and can generate different sag profiles, both balanced and unbalanced, simulating three-phase and phase-to-phase faults respectively, as shown in Section 3. The IUT will be controlled in order to provide rated power at rated AC voltage and also to react as required by standards in case of voltage sags.

Once the DC link has been charged, the voltage sag generator is activated to create the necessary three-phase AC voltage. When the IUT detects connection conditions, it starts its synchronization process. Then, an active power reference is set to the control of the IUT so that the test can take place with the required power generation, typically full-load and low-load tests. In the case of BDEW, [29] states that tests must be carried out at two active power ranges in accordance with [30], the low-load test being between 10% and 30% of rated power and the full-load test at over 90% of rated power. When the system reaches its steady state, a voltage sag command is fed into the control of the voltage sag generator (VSG). A voltage sag appears at the IUT terminals and its LVRT process starts. After the sag, the system returns to its previous state, ready to ride through a new voltage sag.

3. The voltage sag generator

An inverter with a LC output filter has been used in order to generate voltage sags. This inverter can be considered as a controlled voltage source so that, in standard operation, it sets both the desired voltage amplitude and frequency. Moreover, it can generate balanced and unbalanced voltage sags.

The voltage phasors of a balanced three-phase system are shown in Fig. 2. Both phase-to-neutral (V_a, V_b, V_c) and phase-to-phase voltages (V_{ab}, V_{bc}, V_{ca}) are depicted in dotted lines. In the case of a three-phase sag, all voltages are simultaneously reduced to a value p times smaller, where p is defined as the per unit remaining voltage during the sag. Consequently, if V is the phase-to-phase RMS voltage, the phase-to-phase remaining voltage during the sag will be pV. In this case, the phase angles do not change, as shown in Fig. 2 in dashed lines. Nevertheless, when an unbalanced voltage sag takes place, not only the voltage amplitude but also the phase angles are affected, as is the case of a phase-to-phase voltage sag between phases A and B [31]. In this case, phase-to-neutral voltage V_c remains unchanged in both amplitude and phase. As V_{ab} changes to pV, V_{bc} and V_{ca} change to qV in order to keep neutral point voltage. Let θ be phase-to-phase voltage supplementary angle and γ and x the angle and the magnitude of phase-to-neutral voltages V_a and V_b, as depicted in bold lines in Fig. 2. Based on their phasor relationships and Kirchhoff's second law and solving for θ, γ, x and q as a function of p, yields

$$\theta = atan\left(\frac{\sqrt{3}}{p}\right) \tag{1}$$

$$\gamma = atan(\sqrt{3}p) \tag{2}$$

$$x = \frac{pV}{2\sin\left(atan(\sqrt{3}p)\right)} \tag{3}$$

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