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Anomaly detection for IGBTs using Mahalanobis distance

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ABSTRACT

In this study, a Mahalanobis distance (MD)-based anomaly detection approach has been evaluated for non-punch through (NPT) and trench field stop (FS) insulated gate bipolar transistors (IGBTs). The IGBTs were subjected to electrical–thermal stress under a resistive load until their failure. Monitored on-state collector–emitter voltage and collector–emitter currents were used as input parameters to calculate MD. The MD values obtained from the healthy data were transformed using a Box–Cox transform, and three standard deviation limits were obtained from the transformed data. The upper three standard deviation limits of the transformed MD healthy data were used as a threshold for anomaly detection. The anomaly detection times obtained by using the MD approach were compared to the detection times obtained by using a fixed percentage change threshold for the on-state collector–emitter voltage.

1. Introduction

Insulated gate bipolar transistors (IGBTs) are the power semiconductor switch of choice for operating voltages above 200 V [1]. Due to their low on-state voltage drop and simple gate drive requirements, IGBTs have been widely used in medium- and high-power motor drives and power supplies. IGBTs have been reported to fail under excessive electrical and thermal stresses in variable speed drives [2] and are considered as reliability problems in wind turbines [3], inverters in hybrid electric vehicles [4], and railway traction motors [5]. To address these reliability issues, there is an increased focus on the development of diagnostic and prognostic techniques for IGBTs.

Anomaly detection approaches have been reported in literature for identifying faults in IGBT power inverters which involve monitoring system level currents and voltages, collector–emitter voltage, gate emitter voltage and collector emitter current for fault diagnosis. These methods have been developed to identify system level faults and the location of the faulty IGBTs and are not meant to detect faults in the IGBTs themselves [2,6]. A prognostic approach was reported for IGBTs in power modules in automotive applications [7]. This approach involved measurement of the IGBT collector–emitter saturation voltage at vehicle start-up and comparison of the measured value to a look-up table that contained healthy values of on-state collector–emitter voltage $V_{CE(ON)}$. A 15% change for $V_{CE(ON)}$ was used as a threshold for anomaly detection. In another study [8], a 7% change in $V_{CE(ON)}$ was proposed as a threshold for anomaly detection for power module failures as a result of wire-bond degradation.

In this study, we present an alternate approach to fault detection in IGBTs which involves the use of Mahalanobis distance (MD) for anomaly detection. One of the advantages of the MD approach is that it can be derived from multiple parameters which could potentially provide earlier anomaly detection times in comparison to using a single parameter. This approach was implemented on data obtained by electrical–thermal stress experiments performed on non-punch through (NPT) and trench field stop (FS) IGBT devices. The $V_{CE(ON)}$, on-state collector–emitter current $I_{CE(ON)}$, and package temperature were monitored in-situ during the test. MD was calculated using $V_{CE(ON)}$ and $I_{CE(ON)}$ parameters, and a threshold was defined to detect anomalies. The detection times obtained by this approach were compared to the detection times obtained by the use of a fixed percentage change threshold for the on-state collector–emitter voltage.

This paper is organized in five sections. Section 2 describes the procedure used to stress the IGBT devices to failure as well as the data obtained from the experiments, Section 3 describes the equations used to calculate MD and the methodology used for determining the thresholds for anomaly detection, Section 4 describes the results, and Section 5 summarizes this work.

2. Experimental procedure

Ten NPT (IRGB15B60KD) IGBTs labeled N1–N10 and FS (IRGB4056) IGBTs labeled F1–F10 from International Rectifier were

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evaluated in this study. A schematic of the NPT and FS IGBT is shown in Fig. 1. The IGBT devices were packaged in a TO-220A package along with a soft recovery diode. The devices were rated for a collector–emitter voltage of 600 V and gate–emitter voltage of 20 V. The maximum junction temperature rating was 150 °C for NPT and 175 °C for FS IGBTs.

The detailed description of the experimental setup used for power cycling of IGBTs is provided in [10]. To perform the IGBT electrical–thermal stress tests, the IGBTs were switched on and off with a gate voltage of 15 V, duty cycle of 50%, switching frequency of 1 kHz, and collector–emitter voltage of 5 V. The switching was performed until the device reached a pre-defined maximum temperature as illustrated in Fig. 2. Once the maximum temperature T_{max} was achieved, switching was stopped until the device cooled to T_{min} after which switching was resumed again. The temperature increase was caused by self-heating of the IGBTs. No external heat source was used. The main contributor to the self-heating was due to conduction losses in comparison to the switching losses as the switching frequency was low (1 kHz). The temperature at the start of the tests was room temperature. T_{mean} in the experiments was set to 300 °C for NPT and 250 °C for FS IGBTs, and the T_{min} and T_{max} temperatures were set to a range of ±15 °C from the mean temperature.

In this stress condition, failures observed were either due to latch-up (loss of gate control leading to increase in collector–emitter current) or failure to turn on. The failure mode and failure times for the devices tested are given in Tables 1 and 2 .

In-situ measurement of the collector–emitter voltage, collector–emitter current, and package temperature was performed every 400 ms until failure of the IGBT under test and recorded using a National Instruments data acquisition system (NI-DAQ). Temperature monitoring was performed using an infrared sensor focused on the front surface of the package, and current measurements were performed by a Hall-effect current sensor. Fig. 3 illustrates the latch-up failure mode observed for an FS IGBT. The current peaks in Fig. 3 represent the current as the IGBT heats up from T_{min} to T_{max}. The current reduces to zero as the IGBT cools down to T_{min} before switching begins again. At latch-up the current exceeded 18 A upon which the collector–emitter voltage supply was cut off to prevent device burn-out.

Periodically during the test, a square gate pulse of magnitude 1.5 times greater than the stress voltage with a 1 ms duration and 50% duty cycle was applied to the gate. The collector–emitter current and collector–emitter voltage responses to this gate pulse were recorded using an oscilloscope as shown in Figs. 4 and 5.

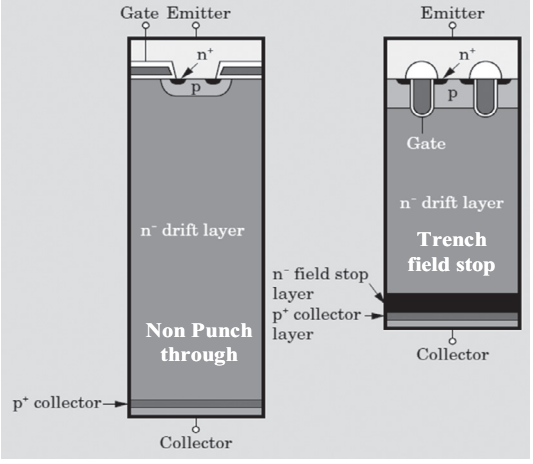

Fig. 1. Schematic of the non-punch through and trench field stop IGBTs [9].

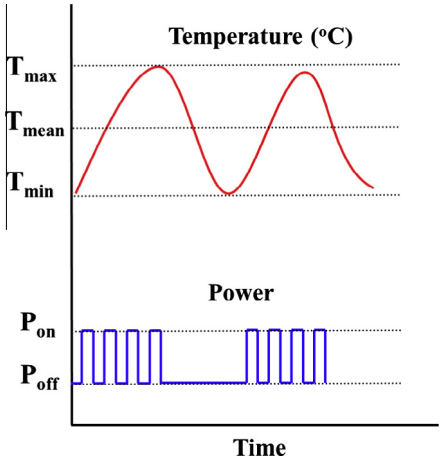

Fig. 2. Schematic of temperature and switching stress profile.

Table 1
Failure time and failure mode for NPT IGBTs.

Device ID	Failure time (min)	Failure mode
N1	47.1	Latch-up
N2	55.8	Failure to turn on
N3	48.7	Latch-up
N4	60.0	Failure to turn on
N5	39.4	Latch-up
N6	56.2	Failure to turn on
N7	42.6	Latch-up
N8	41.0	Latch-up
N9	54.8	Latch-up
N10	34.8	Latch-up

Table 2
Failure time and failure mode for FS IGBTs.

Device ID	Failure time (min)	Failure mode
F1	36.8	Latch-up
F2	51.0	Latch-up
F3	39.5	Latch-up
F4	24.6	Latch-up
F5	56.2	Latch-up
F6	58.2	Latch-up
F7	61.0	Failure to turn on
F8	42.7	Latch-up
F9	56.7	Latch-up
F10	52.6	Latch-up

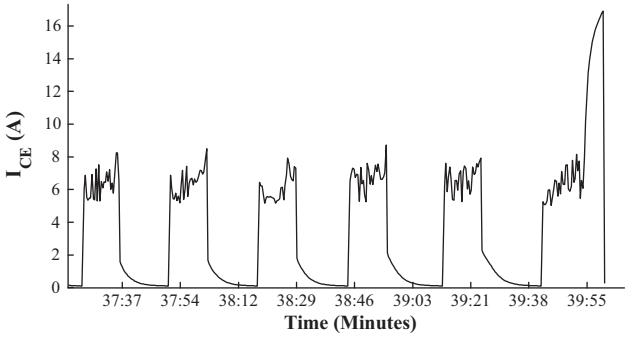

Fig. 3. Latch-up of FS IGBT (F3) as recorded using the NI-DAQ.

To determine the effects of the electrical–thermal stress without the influence of temperature changes, the collector–emitter voltages and currents at the mean test temperature were extracted