



An analytical model for the performance evaluation of multistage interconnection networks with two class priorities

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ABSTRACT

The aim of this paper is to develop an analytical method for performance evaluation of double prioritized Multistage Interconnected Networks (MINs) with single or multilayers and backpressure operation which provide service differentiation and QoS guarantee to an end application running over next generation Internet or Grid systems. Specifically, a new architecture of switching elements is used for the construction of MINs. This switch element uses two parallel queues in order to serve dual priority traffic. Besides this, uniform traffic conditions are presupposed and the bulk of packet arrivals in each cycle to the network inputs follow a Bernoulli distribution. A new analytical model for evaluating single buffered MIN's with 2×2 special switching elements supporting internally two classes' priority traffic is presented. Equations for the steady state are derived. These equations are then used in finding the most important multistage network performance metrics, such as throughput, and packet latency. The results are also validated using simulation and compared with previous related work in marginal cases. This proposed analytical model is accurate for various network sizes and various values of offered traffic to the multistage network inputs.

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1. Introduction

Multistage Interconnection Networks (MINs) with the Banyan property [1–3] are networks where a unique path from an input to an output exists. Such MINs of size $N \times N$ (N inputs and N outputs) consist in general of $k \times k$ Switching Elements (SEs of k inputs and k outputs) [4,5]. High performance is the most important factor in designing MINs. Therefore, effective evaluation techniques are important in order to compare various architectures for their performance.

With the rapid emergence of modern Internet applications, efforts are underway to provide Quality of Service (QoS) to Internet or Grid systems. One possible way of doing this is to assign a higher service priority to real-time traffic (such as video or voice) over non-real-time traffic (such as data). Such QoS cases have been proposed in [6–8].

The two-class priority MINs can be used to face the demand of QoS, especially on supporting both voice and data traffic co-instantaneously. In this study we work on a new architecture of

SE which uses parallel queues in order to achieve the demands of QoS. Those two-class priority MINs have the ability to multiplex data with any real-time traffic, such as e.g. the continuous-bit-rate (CBR) voice traffic. This special type of traffic arises when fixed rate coders are used to compress voice sources. Such traffic can also arise at the edge of a broadband network which is connected to existing circuit switched systems. In real networks, it is expected that a substantial amount of traffic will be of the continuous-bit-rate type and will be offered by existing circuit-switched sub-networks.

In order to estimate the performance of the above mentioned MINs supporting two-class priority, besides the real measurements of an existing system, analytical methods and simulation can be used. Real measurement suffers from high cost, self-interference and overhead. On the other hand the classical simulation is a time consuming process.

In this paper, a new analytical method is developed and simulation is used for confirmation of the results.

The analytical model is based on describing the discrete time behavior of the system. We use utilization formulas of the steady state of the MIN.

Considering the previous work relevant to this topic, Bouras et al. [6,7], analyzed Banyan networks with finite buffers, providing the solution of the steady state distribution of the first stage. They

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also approximated the solution for the subsequent stages, and presented the exact solution for all stages of MINs with unbuffered switches. The same authors in [9] extend their study and give a solution regarding the queuing delay in different types of MINs. Also some new methods are presented in [10].

Also, Markov chains have been extensively used by many researchers such as e.g. Bolch et al. [11]. Bolch et al. used Markov chains in order to approximate the behaviour of MINs under different buffering schemes. [12] by Garofalakis et al., and Tutsch et al. [13] are typical examples of applying analytical techniques on multistage networks.

In addition to that, some solutions using classic simulation are presented by Vasiliadis et al. [14], Tutsch et al. [15] and Miguel-Alonso's group in [16].

Besides the above methods (analytical and simulation), in the literature there is another alternative method based on Petri nets modeling for performance evaluation of MINs. German in [17] is one such approach.

All the above mentioned works are related with single priority MINs. Nevertheless, traffic priority is today a common issue in networks. Traffic with real-time requirements (i.e. VoIP) and traffic of non-real-time applications (i.e. file transfer) are typical examples of such requirements. In the market there are already some switches that accommodate traffic priority possibilities, such as [18,19]. In addition, the SEs used in the [18–21] commercial switches, employ two-class priority services.

Dewar et al. [22] introduce a simple modification to load-sharing replicated buffered Banyan networks to guarantee priority traffic transmission. Finally Chrysos et al. [23] deal with dual priority MINs working on a different SE architecture that we examine in this paper. Looking into the literature for relevant studies to service MIN with priority, we notice some relevant efforts. Firstly, Shabtai et al. [24], study a relevant architecture introducing an approach of a long Markovian memory performance model under uniform traffic. Also an interesting mathematical approach presented by Nassar et al. in [25] and Garofalakis et al. in [26,27].

All the above mentioned papers except [23–25] were studies on single priority fabrics with controlled inputs. On the other hand, this paper deals with internal two-class priority switch fabric architectures and focuses on the impact of this specific architecture on the MIN's performance under two-class priority traffic. A new analytical model for performance evaluation is developed, assuming uniform traffic and Bernoulli type arrivals on the MIN's inputs. Numerical results and a short discussion are presented.

Eventually, the contribution of this paper can be summarized by the following points:

- A new SE architecture is used for our analysis and performance evaluation. Thus, the results can be useful in the industrial area or by network designers.
- Second, a novel approach is presented taking into account only 2 and 3 states for High and Low priority respectively. This consideration leads us to have a better approach to the steady state solution.
- Third, our new analytical method converges very fast and gives accurate results in a small number of iterations, in comparison with simulations which are more time-consuming processes as for all simulation experiments. This approach is a very useful tool in studying QoS matters on communications links that support simultaneously both voice and data traffic.
- Moreover, this model is applied to multilayer MINs when they support a double prioritized traffic schema providing the necessary service differentiation needed by future QoS networks.

The results obtained from both the analytical model and simulation experiments were found to be in close agreement (differences were smaller than 2%), which is evidence of the accuracy of our analytical method.

Organization. The paper is organized as follows: Section 2 presents briefly the description and operation of MINs and focuses on the multistage networks with two-class priority supporting SEs. The 2×2 special SEs contain the special construction with two internal parallel buffers. Section 3 presents some definitions of performance metrics for MIN and furthermore presents some definitions and lemmas related to internal queues as well as some assumptions necessary for our experiments. In Section 4, the analytical method is presented. From our analysis we extract the approximate analytical formulas referring to high and low priority queues respectively.

In Section 5 (and the appendices), we present the methodology of calculating the steady state utilization by applying a convergence algorithm for evaluating the most important performance factors (throughput and packet latency). Section 6 contains some results of our analytical approximation scheme for different network size MINs with various ratios of high priority traffic over the overall offered traffic on MIN's inputs. Section 7 presents results which are related with multilayer MINs. Finally, Section 8 concludes with a short summary and an outlook on future work.

2. MINs description

2.1. General background of MINs

MINs are typical multistage self-routing switching fabrics (e.g. in Fig. 1). They provide a single path between any input–output pair. Self-routing switching means that every SE accepting a packet in one of its input ports can decide in which of its output ports to forward the packet, depending only on the destination address (Fig. 1).

The construction of MINs follows the following general rules:

1. The $N \times N$ MIN switch consists of $L = \log_2 N$ stages, numbered from 1 to L .
2. The MIN is constructed by a total of $\frac{2}{N} \log_2 N$ Switching Elements (SEs).
3. The basic SE is a $k \times k$ (usually $k = 2$) crossbar switch.
4. Switches are connected by unidirectional lines.
5. The switches have a FIFO policy for their servers (outputs). Conflicts between packets simultaneously routed to the same output port are resolved by holding one packet in a queue and servicing the rest.

Packets arrivals to each input of the network are governed by a typical Bernoulli process; thus the probability of packet arrivals to MIN inputs within a clock cycle, are constant and independent of each other.

Regarding the forwarding process, only one packet can be sent to the next stage queues in a time cycle by a SE. The packets are uniformly distributed across all the destinations.

In addition, we incorporate in our analysis the phenomenon of blocking. Blocking situations occur when the packets compete for a full output port of a next stage switch or when the packets face a contention in order to occupy a position in the next queue. This consideration is a realistic view of their operation.

All the arriving packets on input ports contain the data to be transferred as far as the routing tag and the priority tag. For achieving synchronously operating SEs, the MIN is internally clocked.

The network fabric is working with two sequence time phases in a clock cycle. In the first time phase of a clock cycle, flow control information passes through the network from the last stage to the

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