Formulation and heuristic algorithms for multi-chip module substrate testing ☆

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ABSTRACT

Multi-chip module (MCM) substrates are designed for packing two or more semiconductor chips. On these substrates, there are open faults in the wiring, which are electrical disconnections. We must therefore test the substrates to detect open faults, and it is essential to establish an efficient method of testing them. One type of test method uses two probes. Two probes, each touching one edge (end) of an inter-chip wiring, are used to check for the presence of faults. Testing is complete when we have confirmed that no faults exist on the MCM substrate. The objective is to minimize the time to complete testing, that is, our aim is to design efficient routes for the two probes. In this paper, we propose a novel approach of formulating the routing problem as a shortest path problem with covering constraints (SPCC) and we also propose three algorithms for the SPCC. In computational experiments, we show that our formulation and algorithms outperform the existing method.

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1. Introduction

Multi-chip module (MCM) substrates are designed for packing two or more semiconductor chips [1,2] and many different chip dies are connected through a wired interconnect on these substrates. The end of a wired interconnect is called a *pin*, and a set of pins that are to be electrically connected is called a *net* (Fig. 1). MCM technology provides dense assembly capabilities and increased chip packaging at relatively low cost [3]. Because of the high-density assembly, MCM has several advantages in terms of power consumption, package volume, and so on [4]. However, high-density assembly causes faults on MCM substrates [5–8]. These faults are classified as *open faults*, *short faults*, *near-open faults*, and *near-short faults* (Fig. 2). An open fault is an electrical disconnection between two points (pins) that are to be connected. A short fault is an electrical connection between two different nets that are not to be connected. A near-open fault is nearly a wire break, but not an electrical disconnection; hence, this fault causes a high-resistance connection. A near-short fault is caused by insufficient spacing between nets (pins); thus, this fault may result in a short fault. In order to detect these faults, we measure the resistance or capacitance in a wire, and the measured value indicates which faults, if any, are present in the wire.

Additionally, due to dense assemblies, each process of producing the MCM substrates takes much time. If one process is too time-consuming, the total time of completion of a MCM substrate is also so large. Hence, all processes need to be efficient. In particular, the checking of the above faults is too time-consuming and it is likely to be a bottleneck in the production of MCM substrates. An efficient method for checking faults therefore needs to be established [9] and it leads to a productivity improvement of MCM substrates. Electron-beam testing and probe testing have been proposed for fault detection. Electron-beam testing injects a charge into the nets and then scans them. The main advantage of this method is that it is adaptable to many substrate layouts without having to shift the hardware. In addition, electron-beam testing avoids a large number of

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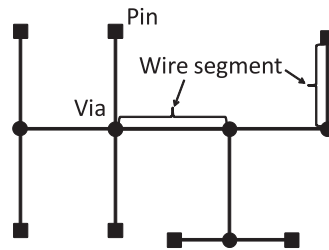 E-mail address: murakami@ise.aoyama.ac.jp

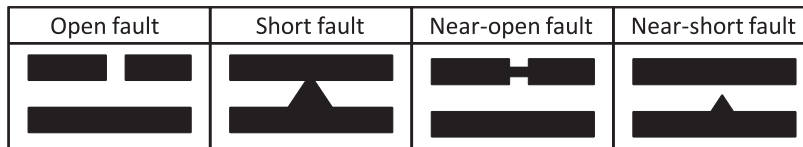Fig. 1. A net with seven-pins configuration.

Fig. 2. Types of substrate faults [13].

mechanical contacts between the testing equipment and the substrate. This method may therefore be used on sensitive pins and fragile substrates. However, the vacuum-based electron-beam system has drawbacks with long testing times and high costs [10]. In contrast, in probe testing, the pins on the substrate are in direct contact with the testing equipment; the equipment is called a *probe*. This method is much faster and less expensive than electron-beam testing. This paper deals with probe testing, in which two probes simultaneously touch two pins, and wiring faults between the two pins are detected [11–16]. We use digital measurements to detect open and short faults, and analog measurements are used for detection of near-open and near-short faults. The analog measurements are usually much slower than the digital ones. Thus, in practice, only open and short fault are considered for probe testing. Furthermore, we can acquire sufficient information on capacitance to detect any short faults, even though we must test all the wires to detect open faults. We therefore usually have only to detect open faults [8].

1.1. Previous studies and our contributions

Several previous studies have proposed probe-testing methods. Yao et al. proposed a method using a two-phase approach with two probes [17]. The first phase produces a set of pairs of pins (for short, a pair set) and the pair set checks all the faults. In the second phase, the routes of the two probes are designed. The second phase corresponds to solving the traveling salesman problem (TSP). They then extended their method from two probes to k probes [4,18]. Kahng et al. [10] and Chu et al. [6] proposed a method for producing minimum pair sets (the size of the pair set is minimum) in the first phase of the two-phase method. Also, Chou et al. proposed an approach that iterates the two-phase method and gradually improves the solution. To our knowledge, all previous studies solved the substrate testing problem using a two-phase method. However, we think that two-phase methods are inadequate because it is too difficult to produce appropriate pair sets in the first phase. When we produce an inappropriate pair set in the first phase, the solution is bad, even if we obtain an optimal route for the probes in the second phase. Yao et al. produced only one pair set and Kahng et al. [11] produced several pair sets in the first phase. They generate a (several) pair set(s) without considering optimization of the probe routes. Hence, the pair set(s) generated may not be appropriate. Kahng et al. and Chou et al. produced only minimum pair sets in the first phase. If there is a net with six pins, the minimum pair set size is three. Minimum pair sets are not always appropriate because if there is a substrate consisting of two nets that have most of their pins on one side (Fig. 3), we should design the probe routes so that one probe
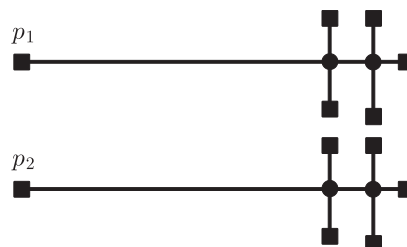

Fig. 3. One-sided nets.