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Fast optimization of nano-CMOS voltage-controlled oscillator using polynomial regression and genetic algorithm

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ABSTRACT

Fast optimization of CMOS circuits is needed to reduce design cycle time and chip cost and to enhance yield. Mature electronic design automation (EDA) tools and well-defined abstraction-levels for digital circuits have largely automated the digital design process. However, analog circuit design and optimization is still not automated. Custom design of analog circuits and slow analog in SPICE has always needed maximum efforts, skills and design cycle time. In this paper, two novel design flows are presented for fast multiobjective optimization of nano-CMOS circuits: actual-value optimization and normalized-value optimization. The design flows consider two characteristics for optimization i.e. power and frequency in a current-starved 50 nm voltage-controlled oscillator (VCO). Accurate polynomial-regression based models have been developed for power (including leakage) and frequency of the VCO to speedup the design optimization. In the actual-value optimization flow, the power model is minimized using genetic algorithm, while treating frequency ≥100 MHz as a constraint. The actual-value optimization flow achieved 21.67% power savings, while maintaining a frequency ≥100 MHz. In the normalized-value optimization flow, the normalized form of these models are subjected to a weighted optimization using genetic algorithm. The normalized-value optimization flow achieved 16.67% power savings, with frequency ≥100 MHz. It is observed that while the actual-value optimization approach provides a better exploration of the design space, the normalized-value optimization approach provides a ≈5× speedup in the computation time.

1. Introduction

Digital design exploration and optimization is highly automated due to availability of large number of electronic design automation (EDA) or computer-aided design (CAD) tools. The digital design automation is aided by the availability of well-defined abstractions for digital circuits (such as system, architecture, and logic levels). However, analog design optimization is still a difficult and time intensive process [1]. For example, the analog simulation time for a nano-CMOS phase-locked loop is a matter of several days. So, debugging such a design is time intensive and costly. This results in high-cost and longer design cycle time. If such analog design are performed at nano-CMOS technology, the issues are further complicated due to leakage and process variation resulting in yield loss.

Most analog integrated circuit (IC) optimization problems involve minimizing a cost function subject to certain constraints. Due to the increasing complexity of modern analog integrated circuits, analog sizing has evolved into a "simulation and optimization" based approach from a "paper and pencil" based approach [2]. Analog sizing problems often require handling multiple conflicting goals, such as power consumption and frequency of a VCO [3]. Novel design/optimization flows are needed, to help the circuit designers [4]. Multi-objective optimization [5] is the process of simultaneously optimizing two or more conflicting design objectives while subjecting the design variables to constraints. During optimization, the baseline design is iteratively tuned by adjusting a large number of design parameters to vast amounts of different design possibilities of the circuit to meet the target design objectives, making it very tedious to do exhaustive design space exploration for complex nano-CMOS circuits to find an optimal solution. Also, the use of compact models [6] with hundreds of parameters in nano-CMOS technology further aggravates the situation.

Polynomial regression model is an abstract model of the netlist which enables a fast design space search. Polynomial regression

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models are useful for relative functions to unknown and very complex non-linear relationship [7,8]. This model is a mathematical predictive equation which may be used as a substitute for the actual circuit, leading to easier and faster simulations with multiple iterations during optimization. For example, as reported in current literature, simulated annealing used on a circuit netlist in a simulator gives convergence in order of minutes as compared to milliseconds, when used over a polynomial regression model [9]. Hence, it can be used as an alternative to the exhaustive search of the design space of the actual circuits. The model can also be used in a variety of tools, such as MATLAB, and is language independent and can be used in a flexible fashion.

To give an overview, the notations and definitions for various terminologies used in this paper are given in Table 1. The paper is organized in the following manner: Contributions of this paper are summarized in Section 2. Section 3 presents the prior related research. Section 4 discusses the proposed novel design flows. The design and analysis of the 50 nm VCO is presented in Section 5. Polynomial models for actual-value and normalized-value optimization are presented in Sections 6 and 7, respectively. Sections 8 and 9 highlight the optimization step of the optimization flows, using genetic algorithm. This is followed by conclusions and future research in Section 10.

2. Contributions of this paper

This paper advances the state-of-the-art in design optimization of analog and mixed-signal circuit where optimization over netlist is time consuming. The *novel contributions* of this paper are as follows:

1. Two novel fast design flows for multiobjective cost function optimization over actual-value and normalized-value in nano-CMOS analog circuits are proposed. The speed up in the design flows is achieved by the use of polynomial regression models and genetic algorithm based algorithms.
2. A method for polynomial regression based modeling has been used for analog circuits. The goodness-of-fit of the polynomial regression models is measured using *SSE*, *RMSE* and R^2.
3. A genetic algorithm based optimization approach is presented that considers power consumption as objective and frequency as constraint for the actual-value optimization approach, and a weighted fitness function for the normalized-value optimization approach.
4. A 50 nm CMOS based current starved VCO is subjected to the proposed design methodology. We report 21.67% power savings and frequency ≥100 MHz using the actual-value optimization flow, and 16.67% power savings and frequency ≥100 MHz in the VCO using the normalized-value optimization flow.

Table 1
Notations and definitions used in this paper.

pwr	Power consumption of VCO
$freq$	Oscillation frequency of VCO
$\widehat{f_{pwr}}$	Normalized polynomial model for power consumption of VCO
$\widehat{f_{freq}}$	Normalized polynomial model for oscillation frequency of VCO
f_{pwr}	Polynomial model for power consumption of VCO
f_{freq}	Polynomial model for oscillation frequency of VCO
RMSE	Root of mean square error
R^2	Coefficient of determination
FF	Fitness function of VCO to be optimized
GA	Genetic algorithm
V_{dd}	Supply voltage of nano-CMOS circuit
V_{in}	Input voltage to nano-CMOS circuit
V_{out}	Output voltage to nano-CMOS circuit
W_p	Width of the PMOS transistor
W_n	Width of the NMOS transistor
$g(x)$	Cost function
$h(x)$	Non-linear inequality constraint

3. Related prior research

Multiobjective optimization problems [10,11] are used wherever optimal decisions need to be taken in the presence of trade-offs between two or more conflicting objectives. For non-trivial multiobjective problems, one cannot identify a single solution that simultaneously optimizes each objective. While searching for solutions, one reaches points such that, when attempting to improve an objective further, other objectives suffer as a result. A comprehensive survey of related works on modeling for analog design has been provided in [12]. The technique for generation of posynomial equation based performance estimation models for analog circuits like multistage amplifiers is described in [13]. An automatic procedure for generation of posynomial models using fitting technique is described in [14]. Other modeling techniques, like Pareto surfaces [15] suffer from the issue of scalability. In order to accommodate a larger design space with a higher number of variables, we may use techniques such as artificial neural networks [16], Takagi–Sugeno neuro-fuzzy logic systems [17], support vector machines based regression [18], Kriging [19] in the proposed design flow instead of polynomial regression. Support vector machine (SVM) has been used for modeling of performance parameters for RF and analog circuits [18,20].

A number of global optimization algorithms are available in current literature for optimization of analog circuits, such as genetic algorithm [10], simulated annealing [19], particle-swarm optimization [21], and artificial bee-colony optimization [22]. These algorithms are particularly effective in finding global optimal or near-optimal solutions, as compared to local optimization techniques like conjugate-gradient. Convex Optimization has been explored in [13] where circuit designs are expressed as posynomial models.

Table 2 shows a comparative perspective among some of the existing optimization flows and proposed optimization flows in the paper. The execution time is highly dependent on the complexity of the circuits involved, and also the algorithm being used. The execution times reported in this paper are comparable with

Table 2
Execution time comparison with existing optimization flows.

Reference	Design	Algorithm	Execution time (s)
Garitselov [23]	LC-VCO	Simulated annealing	1.22
Okobiah [24]	Sense amplifier	Ant colony	1.36
Zheng [25]	Folded cascode Op-amp	Cuckoo search	2.6
This paper—actual-value optimization	21-stage current starved VCO	Genetic algorithm	2.99
This paper—normalized-value optimization	21-stage current starved VCO	Genetic algorithm	0.6