Integrated on-chip solid state capacitor based on vertically aligned carbon nanofibers, grown using a CMOS temperature compatible process

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ABSTRACT

Complete miniaturized on-chip integrated solid-state capacitors have been fabricated based on conformal coating of vertically aligned carbon nanofibers (VACNFs), using a CMOS temperature compatible micro-fabrication processes. The 5 µm long VACNFs, operating as electrode, are grown on a silicon substrate and conformally coated by aluminum oxide dielectric using atomic layer deposition (ALD) technique. The areal (footprint) capacitance density value of 11–15 nF/mm² is realized with high reproducibility. The CMOS temperature compatible microfabrication, ultra-low profile (less than 7 µm thickness) and high capacitance density would enables direct integration of micro energy storage devices on the active CMOS chip, multi-chip package and passives on silicon or glass interposer. A model is developed to calculate the surface area of VACNFs and the effective capacitance from the devices. It is thereby shown that 71% of surface area of the VACNFs has contributed to the measured capacitance, and by using the entire area the capacitance can potentially be increased.

1. Introduction

The public demand to have even smarter, thin, small and lightweight electronic devices with enhanced performance and data processing speed requires further miniaturization of micro-devices and also more devices on the active CMOS chip. Technologically, it translates to a need for high energy density capacitors integrated directly on CMOS chip to power up on-chip devices, and for decoupling purposes with minimized current path.

In fact, the industry is currently deploying 3-D and 2.5-D integration technologies containing devices including energy sources on passive silicon or glass interposer which are required to power up the devices present on the CMOS chip or interposer.

In addition, the simultaneous switching of the devices on the chip draws high current, which results in the drop of power supply voltage below the threshold level, creating ripples in the power. Therefore, decoupling capacitors are used which compensate the voltage by releasing energy when the voltage drops below the tolerable level. Moreover these capacitors can also bypass the high frequency noise. The decoupling capacitors should be mounted close to the power terminals of the devices to minimize the current path for better efficiency [1]. In fact, the long current path generates an equivalent series inductance (ESL), which generates impedance variation in power delivery causing the capacitor to be less effective.

Electrochemical double layer capacitors (EDLC), also called supercapacitors, are good candidates because of their high areal specific capacitance [2]. High surface area, conductive and chemically inert materials such as carbon nanomaterials [3] are used as electrode materials in the supercapacitor, and liquid or sol-gel electrolytes as source of ions [4]. The energy is stored by physical adsorption of ions at the surface of electrode materials creating a very thin (a few angstrom) layer of dielectric, thus providing high specific capacitance and long cycle-life (approx. 1 million). However, the liquid electrolytes are often toxic and corrosive, and their integration directly on CMOS chips presents a big challenge. Solid polymer-gel electrolytes based supercapacitors have potential for direct integration on the chip in which the electrolyte and electrode materials are embedded inside the gel thus creating a packaging of supercapacitor. The physical separation of the electrodes helps to eliminate the need of separator materials however the electrolytes face low ionic conductivity problem at room temperature [4].

On the other hand, traditional parallel plate capacitor architecture combined with thin (few nm in thickness) solid dielectric layer and high surface area electrode can also give high areal capacitance at particular footprint area. High areal specific capacitance 58 nF/mm² was achieved by making deep trenches in silicon [5]. Both the insulator to isolate the substrate from the capacitor and the dielectric materials are deposited by LPCVD technique. However, the trenches are fabricated using Bosch
process, which is time consuming, expensive and also irreversible if any problem occurs during trenches fabrication. Moreover, deep trenches in the silicon substrate make the chip mechanically weaker and vulnerable to defects due to warpage. The atomic layer deposition (ALD) is another technique to deposit dielectric which deposits materials layer by layer giving better step coverage, morphology and textures of the deposited film. The ALD technique can enhance the capacitance by utilizing the surface area inside the small pores. The specific capacitance of 440 nF/mm² is achieved from the deep trenches by depositing aluminum oxide (Al₂O₃) dielectric and titanium nitride (TiN) top metal using ALD technique in multilayer capacitor [6]. Multi-layer capacitors are also made in trenches with an improved LPCVD method, and even higher specific capacitance 527 nF/mm² is obtained [7]. Recently IPU (now Murata) has shown 500 nF/mm² capacitor integrated in the silicon interposer with minimum die thickness 100 μm [8].

Carbon nanostructures are also investigated to make solid state capacitor, in combination to the deposition of thin dielectric layer using ALD. However the temperature growth of the carbon nanotubes prevents their direct growth on CMOS chip whereas the transfer process of the carbon nanostructures is traditionally well above CMOS compatible temperature. For example, the carbon nanotubes (CNTs) were first grown at 700–750 °C on silicon substrate and then transferred on the desired substrate. The dielectric thickness of 15–40 nm gives specific capacitance of ~120 nF/mm² at 100–10 kHz frequency [9]. The shorter CNTs (ca. 2 μm in length) grown at lower temperature 500 °C were also used to make capacitor in which both the Al₂O₃ dielectric and TiN top metal of thickness 15 nm each were deposited by ALD. The specific capacitance value was high ~ 42 nF/mm² however the original device size (0.0025 mm²) was small and corresponding capacitance (106 pF) was not practical [10].

In the present work, solid state capacitors based on vertically aligned carbon nanofibers (VACNFs) that can be grown directly on the active CMOS chip and hence integrated, are demonstrated [11]. The fabrication can be carried out using a proven CMOS compatible process [12]. The specific capacitance 10–15 nF/mm² is obtained at 1 kHz frequency.

2. Experiments

A complete fabrication of on-chip integrated dielectric solid state capacitor is shown in Fig. 1. A 4-in. oxidized (500 nm SiO₂) p-type silicon wafer was used as a substrate. The bottom current collector (CC) including a probing pad was defined by photolithography, followed by a sputtered metal stack of Ti/Au (20/50 nm in thicknesses) and lift-off. The metal catalyst, required to grow carbon nanofibers, was then deposited using electron beam evaporation. Vertically aligned CNFs are grown on the bottom current collector using a direct current plasma enhanced chemical vapor deposition (DC-PECVD) method at a monitored sample temperature of 390 °C and a plasma current of 300 mA, similar to [13]. A combination of acetylene and ammonia gas was used for growth of the VACNFs where the acetylene is a carbon source and ammonia is a carrier gas which also etches back the amorphous carbon. Thermal ALD technique was used for conformal coating of dielectric Al₂O₃ on VACNFs. The precursor trimethylaluminium (TMA) and water were used to deposit 50 nm thick layer of Al₂O₃ at substrate temperature of 300 °C at a pressure of 80 mtorr and a pulsing/purging rate of 20/500 ms, Fig. 1d. To define the top electrode, a stack of metals Ti/Au (30/1000 nm in thickness) was sputtered followed by photolithography leaving the resist at the top electrode location. Finally the bare Titanium/gold layers are etched away by wet and dry etching technique, Fig. 1e. The intended capacitance to be measured is shown in Fig. 2a, however the thick oxide between the probe pads and the silicon substrate can build capacitors connected in series, which could be the potential source of parasitic capacitance, Fig. 2b. To measure the parasitic capacitance of the formed capacitor, capacitors of different dimensions are fabricated. By extrapolating capacitance vs area plot, the parasitic capacitance can be extracted. The basic reference parallel plate capacitors without carbon nanofibers are also fabricated for comparison.

The scanning electron microscopy (SEM) analysis of VACNFs after growth and dielectric coating was performed using JEOL JSM-6301F. The images were taken at 40° tilt angle to see the morphology, and to measure the length of VACNFs. Finally, the capacitance of the capacitor was measured at 1 kHz frequency using a LCR meter coupled to two tungsten probes, one of which punched though the ALD layer to contact the bottom electrode.

3. Results and discussion

The tilted view SEM images show that CNTs are different both in length and shape, Fig. 3a. The thin CNTs are sparse with length 4.6–5 μm, however the lengths of shorter CNTs are 1.9–2.3 μm. The ALD deposition of Al₂O₃ shows that dielectric is coated homogeneously and uniformly, without damaging both CNTs and dielectric, Fig. 3b, also previously shown using HRTEM [14]. The top view of the CNTs after dielectric coating and top metal coating clearly show the difference in the diameters, Fig. 3c. Fig. 4a shows the SEM image of a complete three dimensional solid state capacitor which is intended to be integrated directly on CMOS chip. Because of the CMOS temperature compatible processing, the layout of the capacitor can easily be tailored without further processing step. Moreover, the profile of the capacitor is less than 7 μm making it an ultra-low profile capacitor which can easily be integrated into multi-chip packages and future interposer technology (see Table 1).

The capacitances measured at 1 kHz frequency for different footprint areas capacitors are given in Fig. 4b. The equivalent parallel resistances, measured by the LCR were typically 1.9 MΩ, indicating a rather suitable conformal (i.e. void-free) deposition of the Al₂O₃. We therefore can see that the capacitance with CNTs is 7–9 times higher than the capacitance of a parallel plate capacitance with the same footprint area showing the real 3D capacitive effect of CNTs. A complete integrated solid state capacitor of capacitance up to 8 nF is fabricated and verified.

In addition, a parasitic capacitance of very small value (185 pF) is observed by extrapolating capacitance Vs capacitor area plot, which could potentially originate from the parasitic capacitor between contact pads or bottom electrode and silicon substrate through the silicon oxide as discussed earlier. To verify that, the parasitic capacitance is from probe pads and silicon substrate is calculated. The dimensions of the single probe pad area 105 μm × 105 μm and there are two dielectric layers of silicon oxide and aluminum oxide with thicknesses around 400 nm and 50 nm respectively and only silicon oxide under second pad, Fig. 2b. All three parasitic capacitors are connected in series resulting in very small capacitance values 121 fF. Furthermore the
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