

The ODYSSEY approach to early simulation-based equivalence checking at ESL level using automatically generated executable transaction-level model

Maziar Goudarzi *, Shaahin Hessabi, Naser MohammadZadeh, Nasim Zainolabedini

Department of Computer Engineering, Sharif University of Technology, Azadi Avenue, Tehran, Iran

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ABSTRACT

Design technology is expected to rise to electronic system-level (ESL). This necessitates new techniques and tools for synthesizing ESL designs and for verifying them before and after ESL synthesis. A promising verification strategy for future very complex designs is to initially verify the design at the highest level of abstraction, and then check the equivalence of the lower level automatically generated models against that initial golden model. We present one such approach to simulation-based functional verification implemented in our ESL design methodology called ODYSSEY. Our ESL synthesis tool generates a transaction-level model (TLM) at TLM level 2 (i.e., design with partial timing) that corresponds to the input ESL design (which is at TLM level 3; i.e., sole functionality without timing). Both the ESL design and its generated TLM model can be simulated on a host machine with corresponding input stimuli to establish their functional equivalence. The TLM is in SystemC, and hence executable, and also models both hardware and software components in C++ to achieve higher simulation speed. We introduce an implementation of a TLM level 2 model that is tailored to our ESL design methodology and apply our approach to a number of benchmarks to evaluate the TLM simulation performance. Experimental results show that the approach suits early validation of the ESL synthesis process since its simulation performance is more than 4 orders of magnitude higher than simulations at lower levels and it is generated early in the design cycle. Also the co-simulation overhead – compared to simulating the original ESL design in C++ – depends on the partitioning quality in terms of communication to computation ratio.

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1. Introduction

Starting the design from higher levels of abstraction is inevitable to excel the designers' productivity [1]. The industry trend has already been toward electronic system-level (ESL) design [2], where software and hardware of the system are co-designed. In such a design flow, the design process starts from an implementation-independent system model that is later partitioned and elaborated to hardware and software components. This elaboration/partitioning, which we hereafter refer to as *ESL synthesis*, is an essential part of ESL design, and furthermore, is difficult to verify since the pre- and post-synthesis models are in different semantic domains; the pre-synthesis model is implementation-independent whereas the post-synthesis model is a heterogeneous combination of *sequential functional* software and *parallel structural* hardware. In

this paper we present our approach to tackle this problem in ODYSSEY project [11].

The International Technology Roadmap for Semiconductors (ITRS) suggests that future design technologies should facilitate verification of the system-under-design much earlier in the design flow to avoid costly design iterations from lower levels [1]. Fig. 1 shows past, present, and envisioned future design system architectures as viewed by ITRS. In the past (left hand side of the figure), only the operations from *register transfer level (RTL)* design down to the final implementation employed *equivalence checking* (look at the *EQ Check* rectangle at the bottom left of the figure) while various tools and multiple design files were generated and used for hardware synthesis; hardware/software partitioning and optimization were also manual tasks accomplished by expert system designers (look at *HW/SW optimization* cloud at middle left of Fig. 1), and moreover, software optimization was a separate process from hardware optimization procedure (see the separate *SW opt* box at left-middle of Fig. 1). At present (middle part of the figure), hardware/software partitioned model is generated from the high-level system model (compare the top parts of *past* and *present* in the figure) which enables some degree of design-space explora-

* Corresponding author. Present address: System LSI Research Center of Kyushu University, Fukuoka, Japan. Tel.: +81 92 847 5193; fax: +81 92 847 5190.

E-mail addresses: goudarzi@sharif.edu (M. Goudarzi), hessabi@sharif.edu (S. Hessabi), naser@ce.sharif.edu (N. MohammadZadeh), n_zainolabedini@ce.sharif.edu (N. Zainolabedini).

tion; furthermore in the hardware optimization process, multiple design files are converged into one efficient data model that removes many tool interoperability issues and enables efficient iterative optimization methodologies during optimizations from RTL level down to the final implementation (look at the bottom-middle of Fig. 1 and compare it to the *past* case). In future (right hand side of the figure), software optimization and hardware/software partitioning and optimization are to be combined with hardware optimization process (look at the bottom of the flow) and more importantly, verification tasks all move to earlier, higher levels of abstraction (look at the box labeled “functional, performance, testability verification” at the top-right of Fig. 1) followed by *equivalence checking* and assertion-driven design optimization (see the third bullet in the text box at bottom-right of Fig. 1). In other words, this vision of ITRS suggests [1] that with the technology move to higher abstraction levels, modern equivalents are sought for the equivalence checking process that is currently done at logic and register transfer level (RTL).

Solutions to this verification and validation problem fall into two main categories of *formal-verification techniques* and *simulation-based techniques* [3,4]; we follow the latter approach. Simulation-based approaches, sometimes instrumented with assertions,

are more popular due to easier use and more intuitiveness. The main concern in such approaches is the simulation speed. Two approaches exist for such simulations [5]: (i) *interpretive simulation* where the simulator, which is already compiled for the host machine, reads in a model of the system-under-simulation and simulates it, and (ii) *compiled simulation* where the model of the system-under-simulation is itself compiled to execute on the host machine and the results of this execution are the simulation results of the system-under-simulation. We follow the latter since compiled simulation provides the highest speed compared to other approaches because its resulting executable is (i) customized to the system-under-simulation and (ii) optimized for the host computer running the simulation. The general idea of compiled simulation of hardware and logic alone [5] and also *compiled co-simulation of software along with hardware* [6,7] are not new and have been extensively reported and used in the literature, however, it is new and required by the technology trend toward system-level design that (i) tailor co-simulation model to the specific needs of ESL design flow, (ii) automatically generate it in the design flow, and (iii) realize ITRS-envisioned verification flow at ESL level; these are important contributions of this work and our experimental results show that they successfully reduce the validation time and

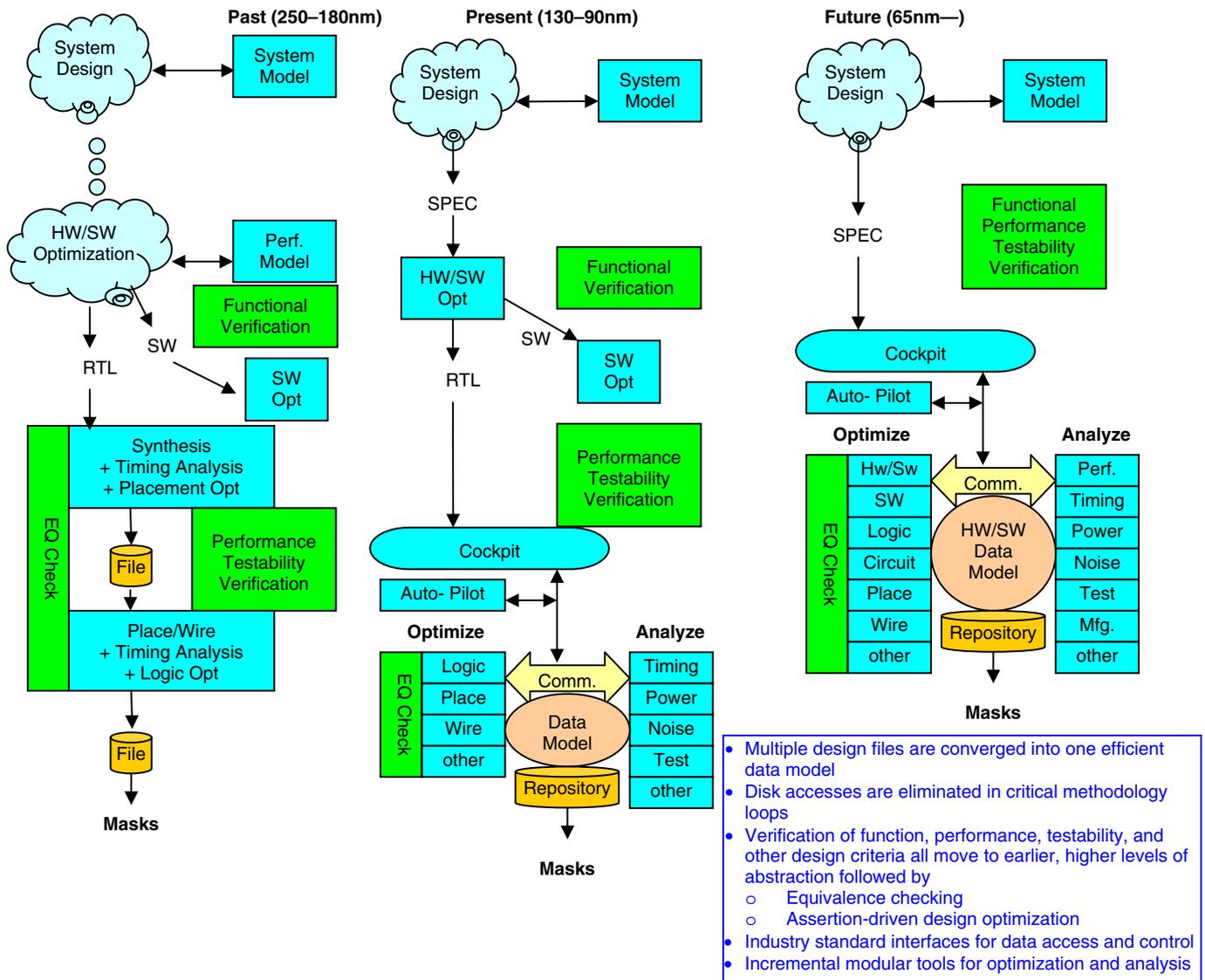


Fig. 1. ITRS-envisioned required evolution of design system architecture [1].

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