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An evolutionary simulation–optimization approach in solving parallel-machine scheduling problems – A case study

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Abstract

Parallel-machine scheduling research is one of the active fields in the past decade due to its increasing application. Due to the problem complexity, it is a general practice to find an appropriate heuristic rather than an optimal solution for the parallel-machine scheduling problem. The wirebonding workstation is the bottleneck in integrated-circuit packaging manufacturing. Effective scheduling is one of the key factors towards improving the efficiency of the wirebonding operations. The wirebonding scheduling problem is an equal (or identical) parallel-machine scheduling problem. The research solved the wirebonding scheduling problem by using an evolutionary simulation–optimization approach. Empirical results, benchmarked against lower bound solutions, showed the quality solutions of less than 2% deviation for a wide range of production scenarios. However, if the problem size were to increase, the proposed methodology might become computationally prohibitive, and this might well require further development if used to solve the identified problem in such circumstances.

Keywords: Discrete-event simulation; Equal parallel-machine; Evolutionary algorithms; Integrated-circuit packaging; Scheduling; Wirebonding

1. Introduction

The manufacture of an integrated-circuit (IC) has three major stages: (i) wafer manufacturing; (ii) wafer processing; and (iii) packaging and final test. In the first stage, wafer is manufactured from high-purity molten silicon. The wafer-processing stage then achieves full integration of the original circuit design onto a die on a wafer, as illustrated in Fig. 1 (Yang & Tseng, 2002). The third stage is discussed in more details as follows since one of its operations is adopted as the case study.

Each die in Fig. 1 represents an individual circuit chip. A finished wafer usually contains 100 to 200 dies, depending on the size of the wafer and the size of the die. A circuit chip must be sealed for mechanical and environmental protection. IC packaging processing separates a die from the wafer, which is then put on a lead frame for a connecting circuit and an application device, as illustrated in Fig. 2(a). Gold wires connect the IC

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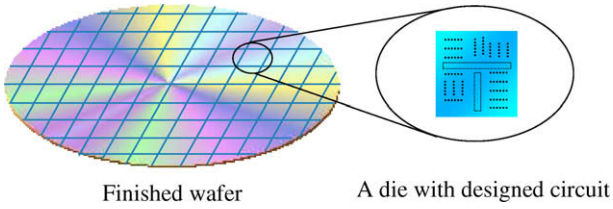

Fig. 1. A finished wafer.

die and the leadframe, as shown in Fig. 2(b). The number of wires required for a specific device usually ranges from ten to thirty. Some sophisticated devices might require more wires. Because the wirebonding process is both time-consuming and cost-effective, it usually has a large number of parallel bonding machines (ranging from tens to hundreds), and it usually represents the bottleneck stage in the IC packaging process. After the wirebonding step, the chip is then encapsulated with plastic, as illustrated in Fig. 2(c). Finally, the chip is separated from the lead frame, and is then tested for its required functions.

Because the wirebonding workstation is usually the bottleneck in IC-packaging manufacturing, it should be the focus of efforts to improve productivity (Gilland, 2002; Harman, 1997; Tovia, Mason, & Ramasami, 2004). An effective scheduling decision is one of the key factors towards improving the efficiency of the wirebonding operations, particularly, for the instance of multiple products. Fig. 3 illustrates the wirebonding system configuration.

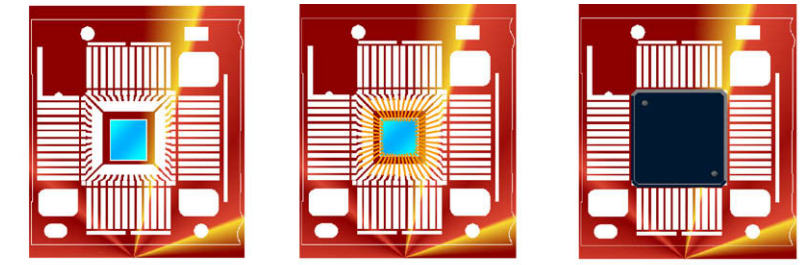

Fig. 2. An encapsulated IC chip.

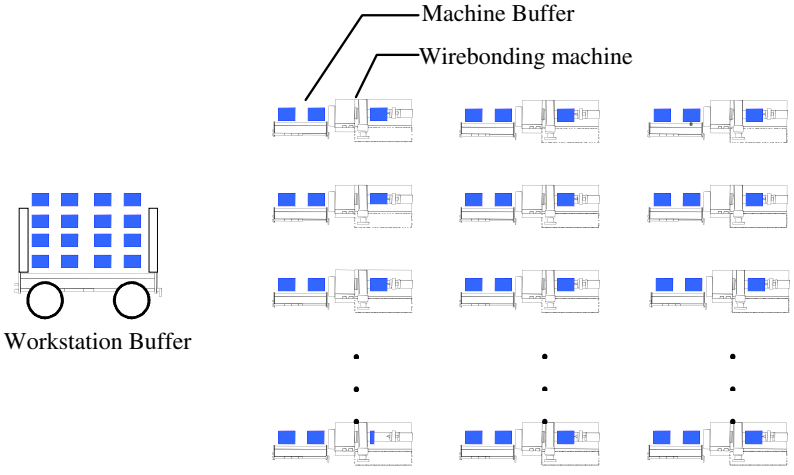

Fig. 3. Wirebonding system configuration.