Available online at www.sciencedirect.com

ScienceDirect

Solid-State Electronics 51 (2007) 611–616

SOLID-STATE ELECTRONICS

www.elsevier.com/locate/sse

Combined sources of intrinsic parameter fluctuations in sub-25 nm generation UTB-SOI MOSFETs: A statistical simulation study

K. Samsudin *, F. Adamu-Lema, A.R. Brown, S. Roy, A. Asenov

Department of Electronics and Electrical Engineering, University of Glasgow, Glasgow G12 8LT, Scotland, UK

The review of this paper was arranged by Simon Deleonibus

Abstract

The ultra thin body (UTB) SOI architecture offers a promising option to extend MOSFET scaling. However, intrinsic parameter fluctuations still remain one of the major challenges for the ultimate scaling and integration of UTB-SOI MOSFETs. In this paper, using 3D statistical numerical simulations, we investigate the impact of random discrete dopants, body thickness variations and line edge roughness on the magnitude of intrinsic parameter fluctuations in UTB-SOI MOSFETs. The sources of intrinsic parameter fluctuations, which can be separated in simulation, will occur simultaneously within a single MOSFET. To understand the impact of these sources of fluctuation in an actual device, simulations with all sources of intrinsic parameter fluctuations acting in combination have also been performed.

Keywords: UTB-SOI; MOSFET; Intrinsic parameter fluctuations; Random discrete dopants; Body thickness variation; Line edge roughness

1. Introduction

With the progressive scaling of conventional MOSFETs to nanometre dimensions, variations in transistor characteristics due to random discrete dopants, interface roughness and line edge roughness start to adversely affect the yield and functionality of circuits constructed from them [1,2]. Due to the scaling limitations of the conventional MOSFETs, novel device architectures, such as UTB-SOI and multi-gate MOSFETs, that are also more resistant to some of the sources of intrinsic parameter fluctuations, are anticipated to play an increasingly important role before the end of the current ITRS [3] roadmap.

UTB-SOI transistors with virtually undoped channels have superior electrostatic integrity and better performance compared with bulk MOSFETs. Working UTB-SOI MOSFETs with a channel length of 6 nm [4] and body thickness down to 3 nm [5] have already been successfully demonstrated. The optimal scaling of the UTB-SOI MOSFETs to such dimensions, however, requires a body thickness in the range of nanometres. At such dimensions, local variations in body thickness, geometry variations, due to line edge roughness and discrete random doping in the source–drain regions, will have a dramatic impact on their characteristic. While UTB devices offer a potential solution to ultimate MOSFET scaling, obtaining reliable initial estimates for the magnitude of their corresponding intrinsic parameter fluctuations becomes extremely important. This work presents a systematic analysis of the intrinsic parameter fluctuations (IPF) in ultimate UTB-SOI MOSFETs using 3D Drift Diffusion 'atomistic' simulations [6]. The UTB-SOI MOSFETs are designed to closely match the requirements of the ITRS [3] for high-performance devices in the 25, 20 and 14 nm technology generation, which correspond to 10, 7.5 and 5 nm channel length devices, respectively.

---

* Corresponding author. Tel.: +44 141 330 2964; fax: +44 141 330 4907. *E-mail address:* K.Samsudin@elec.gla.ac.uk (K. Samsudin).

0038-1101/$ - see front matter © 2007 Published by Elsevier Ltd.
doi:10.1016/j.sse.2007.02.022

2. Simulation methodology

The idealised generic structure of the simulated undoped square channel UTB-SOI MOSFETs is illustrated in Fig. 1. Transistors with channel lengths of 10, 7.5 and 5 nm have been studied. The corresponding equivalent oxide thicknesses are 0.67, 0.5 and 0.33 nm, respectively and associated body thicknesses are 2.5, 2.25 and 2 nm. The doping concentration in the source–drain regions is $2 \times 10^{20}\,\mathrm{cm}^{-3}$ and the threshold voltage was adjusted by a suitable choice of the gate work function (approximately 4.6 eV in each case).

The simulations have been carried out with the 3D Glasgow 'atomistic' drift diffusion simulator [6]. It includes density gradient quantum corrections and can include random discrete dopants (RDD), body thickness variation (BTV) and line edge roughness (LER) as sources of intrinsic parameter fluctuations. The simulation of intrinsic parameter fluctuations shifts the paradigm of traditional device simulation in the statistical domain. In the presence of atomic variations from device to device. It becomes necessary to simulate a statistically significant sample of devices in order to characterize all macroscopically similar but microscopically different devices. An ensemble of 200 macroscopically identical, but microscopically different devices were simulated for each channel length and each source of intrinsic parameter fluctuation individually and in combination to capture statistical variation in the device parameters. At this stage the simulations only capture fluctuations induced by the electrostatics and quantum confinement effect, and do not include mobility variations, or tunnelling through the gate oxide which may be significant for very thin gate insulators.

2.1. Random discrete dopants (RDD)

One of the major advantage of the UTB-SOI devices is the tolerance to very low doping concentrations in the channel. However, unavoidable random discrete dopants in the source–drain regions result in nanometer scale variations of the effective channel length. Variation of the source–drain access resistance due to statistical fluctuation in the number and position of dopant atoms in these same regions may also contribute to the variations of drive current.

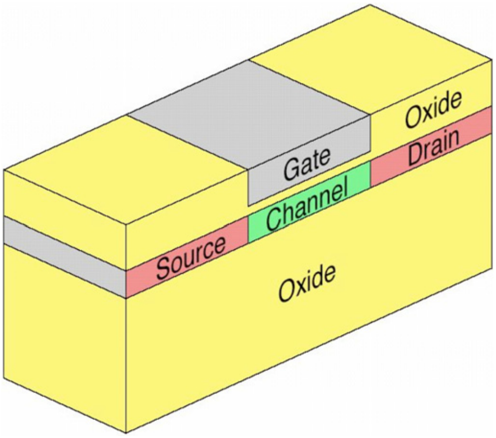

Fig. 1. Schematic view of the UTB-SOI MOSFET simulated in this work.

The most realistic way to introduce the microscopic source–drain doping distributions into the atomistic simulations in an attempt to capture the physics of these processes would be to use the output from an atomic scale process simulator [7,8]. However, here we apply a simpler approach, randomly placing the individual discrete dopants in the source–drain regions of the 3D device simulation domain using a rejection technique based on the continuous doping profiles [6].

A typical potential distribution obtained from RDD simulation of a 10 nm UTB-SOI MOSFET is illustrated in Fig. 2a. The heavily doped source and drain regions are clearly visible in the potential landscape. Strong potential fluctuations at the source–drain and channel interface associated with the discrete dopants placed on average 1–2 nm apart can be observed. The equi-concentration contour in Fig. 2b highlights the basic features of the discrete dopants in the source–drain region. The discrete dopants make the concept of a metallurgical junction obsolete, introducing variation of the effective channel length across the width of each simulated UTB-SOI MOSFET. Although the fluctuations in a conventional bulk MOSFET parameters are dominated by the randomness of dopants in the middle of the channel region [9], atomistic doping in the source and drain of UTB-SOI will introduce variations in the effective channel length, even for a perfectly defined gate pattern.

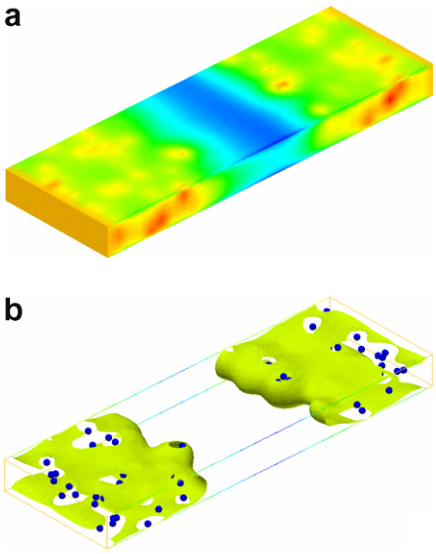

Fig. 2. A typical simulation domain for a 10 × 10 nm gate UTB-SOI MOSFET due to random discrete dopants at threshold. The gate and buried oxide is removed to show the fluctuations in (a) electrostatic potential and (b) carrier concentration contour at the source–drain and channel interfaces and the location of random discrete dopants in the source–drain regions.