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Adhesive wafer bonding with ultra-thin intermediate polymer layers

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ABSTRACT

Wafer bonding methods with ultra-thin intermediate bonding layers are critically important in heterogeneous 3D integration technologies for many NEMS and photonic device applications. A promising wafer bonding approach for 3D integration is adhesive bonding. So far however, adhesive bonding processes relied on relatively thick intermediate adhesive layers. In this paper, we present an adhesive wafer bonding process using an ultra-thin intermediate adhesive layer with sub-200 nm thickness. We demonstrate adhesive bonding of silicon wafers with a near perfect bonding yield of >99% and achieve less than ±10% non-uniformity of the intermediate layer thickness across an entire 100 mm-diameter wafer. A bond strength of 4.8 MPa was measured for our polymer adhesive, which is considerably higher than previously reported for other ultra-thin film adhesives. Additionally, the adhesive polymer used in the proposed method features excellent chemical and mechanical stability. We also report on a potential strategy for mitigating the formation of micro-voids in the polymer adhesive at the bond interface. Furthermore, the polymer adhesive can be sacrificially removed by oxygen plasma etching for both isotropic and anisotropic release etching. The characteristics of the adhesive wafer bonding process and its compatibility with CMOS wafers, makes it very attractive for heterogeneous 3D integration processes targeted at CMOS-integrated NEMS and photonic devices.

1. Introduction

Heterogeneous 3D integration of nano-electromechanical systems (NEMS) and photonic devices on top of integrated circuits (ICs) is an emerging technology which will lead to highly compact devices that combine traditional ICs with advanced sensor and actuator systems. Different components, such as NEMS, photonics, and complementary metal oxide semiconductor (CMOS) circuits are fabricated on separate substrates and subsequently joined into one single substrate, which is typically achieved through wafer bonding [1–3]. This enables the integration of high-performance NEMS and photonic materials such as mono-crystalline silicon or III–V materials directly on top of ICs, which is otherwise not possible. For many of these applications wafer bonding with an ultra-thin intermediate bonding layer is highly desired, which however remains a challenge. Utilizing ultra-thin intermediate bonding layers offers extremely short interconnecting vias between the NEMS structures and the underlying ICs, which improves the device performance and increases the integration density. Shorter vias also allow for smaller via diameters, thus reducing the overall device and system footprint. For photonic applications, ultra-thin intermediate bonding layers are particularly important for integration of III–V materials on top of silicon photonics such as silicon waveguide structures, to achieve good optical coupling and thermal conductance between the III–V materials and the underlying substrate [4,5].

Typical thin-film bonding methods such as anodic bonding [6,7] and eutectic bonding [8,9] are generally not compatible with heterogeneous 3D integration involving CMOS-based ICs, since they rely on high bonding temperatures or high voltages. Low-temperature plasma activated fusion bonding [10–12] and hybrid metal/fusion bonding [13–16] approaches have been developed for 3D ICs and back-side illuminated CMOS imaging sensors. These approaches typically utilize dielectric materials, such as silicon oxide, to form ultra-thin intermediate bonding layers, or dielectric layers with embedded metal areas to form electrically conductive vias. However, fusion bonding methods pose extremely high requirements on the cleanliness and roughness of the wafer surfaces to achieve successful bonding, with potentially negative impact on process yield. In many heterogeneous NEMS integration processes it is required to selectively remove the intermediate bonding layer to release suspended NEMS structures [2,3]. Inorganic intermediate bonding layers such as silicon oxide can be challenging to remove with high material selectivity and can cause

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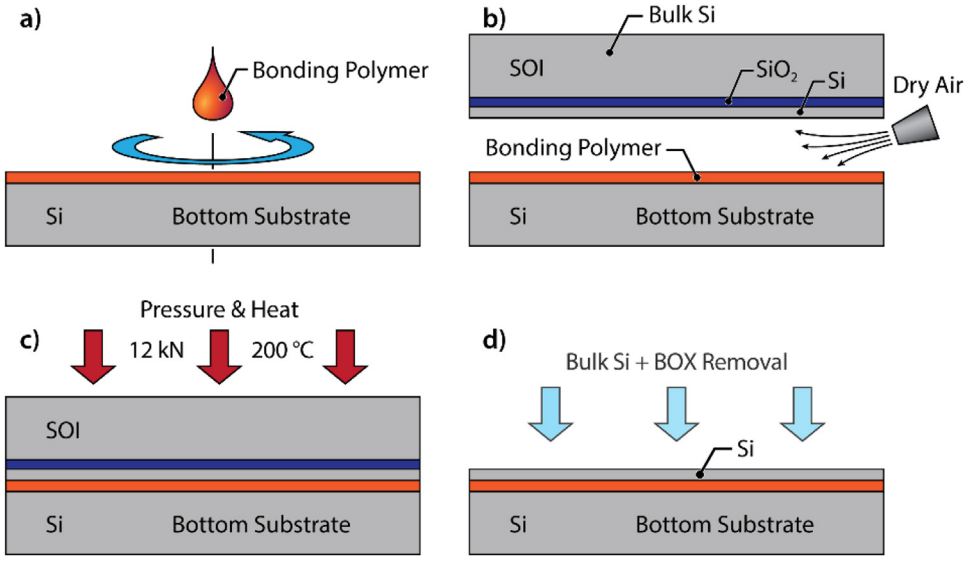

Fig. 1. Adhesive wafer bonding process: a) Spin-coating of 200 nm-thick polymer adhesive layer on the bottom substrate and solvent evaporation at 110 °C for 2 min. b) Dry air cleaning of both bond surfaces and placement of an SOI wafer face down on top of the bottom substrate. c) Thermocompression bonding step by applying a force of 12 kN and a temperature of 200 °C for 50 min. d) Optional thinning of the SOI wafer for inspecting the bond interface, by removing the bulk silicon using reactive ion etching (RIE) and the buried oxide using buffered hydrofluoric acid (BHF).

stiction issues. Other low-temperature bonding methods including thermocompression bonding of metal layers such as gold or copper films [17–20] offer good compatibility with most NEMS and IC materials, however they typically employ relatively thick intermediate bonding layers.

For photonic applications, transfer bonding of III–V materials is most commonly performed by low-temperature SiO_2 direct bonding [21–23] or by adhesive bonding using benzocyclobutene (BCB) [24–28]. So far, low-temperature SiO_2 direct bonding and adhesive bonding with ultra-thin intermediate layers have only been reported for small bonding areas and are thus only suitable for chip-level integration [29,30]. Keyvaninia et al. [31] demonstrated a sub-50 nm intermediate layer for adhesive bonding on a 50 mm-diameter bonding area using divinylsiloxane-diluted BCB. However, using BCB as an adhesive layer poses significant process limitations, since fully cured BCB is extremely difficult to sacrificially etch with good selectively towards the common semiconductor materials, which is crucial for many NEMS heterogeneous 3D integration processes. Thus, there is a clear need for reliable wafer-scale adhesive bonding processes featuring ultra-thin intermediate polymer adhesive layers, adequate bond strength, and a low bonding temperature. In this paper, we address all the above-mentioned shortcomings by proposing a reliable adhesive wafer bonding process using sub-200 nm thick layers of a thermosetting polymer as intermediate adhesive. We demonstrate the viability of this process for 100 mm-diameter wafer-scale processing, by studying the bonding yield, the uniformity of the intermediate bonding layer, the bond strength, and the capability to sacrificially remove the polymer adhesive with a high-selectivity etching process. Thus confirming, that the proposed adhesive wafer bonding process is a very attractive approach for heterogeneous 3D integration platforms targeted at NEMS and photonic applications.

2. Description of the adhesive wafer bonding process

The adhesive wafer bonding process presented in this paper consists of two steps: first, the application of an ultra-thin film of polymer adhesive on one of the two wafers and second, a low-temperature thermocompression bonding step to join the two wafers and cure the polymer adhesive. The thin-film polymer adhesive used for this process is the mr-I 9020 XP thermosetting nano-imprint resist (Micro-resist Technology, Germany) which was chosen for its excellent bonding characteristics as well as mechanical, chemical, and thermal stability up to 300 °C [32,33]. However, our bonding approach is not limited to this particular polymer and can be adapted for many types of adhesives. Due to the simplicity and low bonding temperature of this process, it is compatible with a wide range of wafer materials, including silicon, silicon oxide, glass, germanium, III–V materials (e.g. GaAs), and fully processed IC wafers. We demonstrated the proposed process by bonding using single-side polished silicon substrates as well as SOI substrates. All process parameters are specifically designed to ensure CMOS compatibility of the entire bonding process.

In Fig. 1, a schematic depiction of the adhesive wafer bonding process is presented. The first step, as shown in Fig. 1a), consists of the application of an ultra-thin layer of mr-I 9020 XP polymer adhesive on the bottom substrate using conventional spin-coating at a spin speed of 3000 rpm for 30 s, which results in a polymer layer thickness of 200 nm. The exact layer thickness can be adjusted by changing the spin speed and the dilution of the polymer. After spin-coating, the bottom wafer is placed on a hotplate at 110 °C for 2 min to evaporate the solvents. Fig. 1b) shows the dry air cleaning step and subsequent placement of the SOI wafer on top of the bottom substrate with the silicon device layer of the SOI wafer facing the bond interface. Prior to the placement of the top wafer a dry air gun is used to clean the surfaces of both wafers, thus removing any particles that could cause bonding defects if they are trapped at the bond interface. The thermocompression bonding step, depicted in Fig. 1c), is subsequently performed using a CB8 Bonder (Süss MicroTec, Germany). A bond force of 12 kN is applied while the temperature is ramped to 200 °C in 1 h, maintained at 200 °C for 50 min, and ramped back down to 50 °C in 1 h, which fully cures the polymer adhesive and concludes the proposed bonding process. To simplify the wafer-scale characterization of the bond interface, the bulk silicon of the SOI wafer is removed as shown in Fig. 1d). The removal of the bulk silicon is achieved by reactive ion etching (RIE), while the buried oxide layer is thereafter removed in a buffered hydrofluoric acid (BHF) wet etching step.