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ScienceDirect

Procedia Engineering 174 (2017) 135 – 144

Procedia Engineering

www.elsevier.com/locate/procedia

2016 Global Congress on Manufacturing and Management

The Influence of Lot Size on Production Performance in Wafer Fabrication Based on Simulation

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Abstract

Semiconductor manufacturing has been a significant change over the past decades. Nevertheless, from production efficiency point of view, it should be argued with validity whether 25-wafer is an adaptive lot size in the future to fulfill the manufacturing processes. In this work, a simulation model to study the relationship between lot size and the performances of wafer fabrication is proposed. Three production performance indices are taken into account in this model including cycle time of products, total throughput and the waiting time of WIP by workstation. Based on the simulation result, it reveals that the cycle time of products is synchronously decreased when the lot size is shrunk. However, the waiting time of WIP is not coincident with lot downsizing. From these results, the model of this study can provide a trend to establish the best lot size to fulfill the current and future wafer fabrication.

Peer-review under responsibility of the organizing committee of the 13th Global Congress on Manufacturing and Management

Keywords: Wafer Fabrication, Lot size, Production performance, Simulation model

1. Introduction

The semiconductor industry is a high technology and capital intensive industry. Due to the characteristics of reentrant, complicated processes, time constraints issues and equipment utilization concerns, the

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Peer-review under responsibility of the organizing committee of the 13th Global Congress on Manufacturing and Management
doi:10.1016/j.proeng.2017.01.180

production management is tougher than other industries and managers are facing many difficulties and challenges [1][2]. Besides, semiconductor manufacturing has been grown to maturity and a significant change over the past decades. For example, the wafer size is from 100mm to 300mm and 450mm in development stage; process technology migrates from 10μm above to 10 nm and the process steps is increased from several hundred steps to more than thousands of steps; the fab scale is increased to more than 100K wafer per month. Moreover, in order to improve the wafer yield, some batch process steps, such as furnace, wet bench, have been changed to mini batch or even to the single wafer process [3]. Although there are so many significant changes in wafer fabrication, the lot size still kept 25-wafer is really an issue should be addressed. Hence, from production efficiency point of view, it should be argued with validity whether 25-wafer is an adaptive lot size in the future to fulfill the more advanced and complicated manufacturing processes.

Based on JIT theory and experiences of production management in other industries, smaller transfer quantity is proved as the best policy to reduce the cycle time of product and increase the throughput [4]. However, due to the different characteristics in wafer fabrication, it is necessary to further study that the advantages of small lot size of wafer fabrication. Generally, the increasing of setup time is the most serious impact of small lot size on production performance. In wafer fabrication, there are some equipment processes which need the setup step, such as the change of mask in photolithography process, pumping down in the vacuum equipment and waiting for batching in furnace and wet bench. There will be lost on the production performance due to the small lot size. Nonetheless, as mentioned above, due to the yield concerned the batch process have been changed to mini batch or even to the single wafer process. Besides, some process limitations, such as time constraints, are getting serious in the advanced technology. Therefore, from production efficiency point of view, it should be argued with validity whether 25-wafer is an adaptive lot size in the future to fulfill the more advanced and complicated manufacturing processes.

In the study, the previous researches relevant to the determination of lot size are discussed in the section 2. The next section introduces the environment and the concepts, the analysis and discussions of simulation result is presented in section 4, and the final is conclusions.

Nomenclature

n	Number of lots in a batch
ls	Lot size (piece)
tol	Tolerance
TP	Processing time of lot which lot size equals lt

2. Literature review

There were many researches focused on the effects of the changes of lot size on production performance in semiconductor manufacturing. Lee [5] proposed a lot sizing decision policy to reduce the total processing time on a critical resource of wafer probe operation in semiconductor manufacturing. Wood [6] suggested that the performance improvement could be achieved by using single wafer processing and tool integration together. In addition, this study also implied that the cycle time reduction can be achieved by smaller lot size. Besides, simulation is a general tool used in the studies of lot size [7][8]. Bonnin *et al.* [9] applied DOE and dynamic simulation to review the front-end steps within a semiconductor manufacturing flow where batching requirements may be replaced by single-wafer or mini-batch alternatives for cycle time improvement.